PGM-HD-2x1-PB

HD/SD-SDI 2x1 Program Switch with
Frame Synchronizer

User manual

Rev. B

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Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
B	1	2015-05-15	MB	Cover page update; DoC removed; no other changes to content
1	0	2012-07-13	TB	New feature, on-screen label.
0	A	2012-07-10	TB	New template. Changed product name and completed DIP descriptions. Added EC Declaration of conformity, referring to tested hardware module.
A	-	2011-05-02	TB	Preliminary release.

Contents

1 Product overview

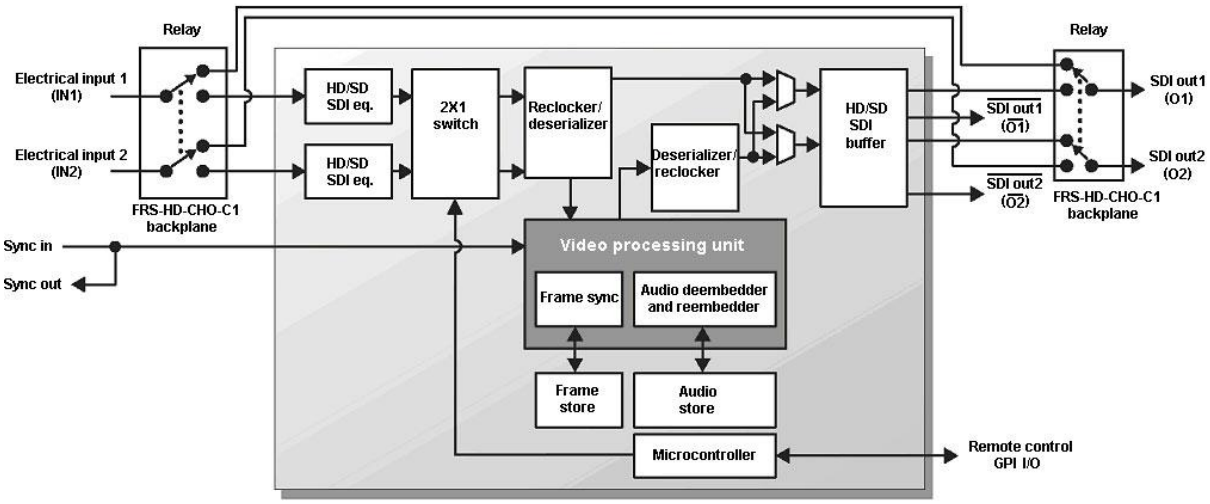


Figure 1: Simplified block diagram of the PGM-HD-2X1-PB card

1.1 Product description

The Flashlink PGM-HD-2X1-PB is a 2x1 HD/SD program switch with configurable fade-in/fade-out and built-in frame synchronizer. Embedded audio is faded in/out with the video. The frame synchronizer locks an HD-SDI or SD-SDI input to a black & burst or tri-level signal, and a de-glitcher ensures an always error-free output.

The user parameters of the card can either be changed by switches on the board, or by the control interface Gyda.

1.1.1 Product versions

At the time of writing this manual, only one version exists, the PGM-HD-2X1-PB.

1.1.2 Key features

- Passive bypass from both inputs to non-inverted outputs with less than 25m loss of cable length (enables full redundancy)
- HD/SD video support (will work with DVB-ASI in through mode, but no fading)
- De-glitching of input video signal (always seamless output)
- Full manual control over selected input or black via GPI inputs or the system controller Multicon
- User selectable generator pattern as fallback for missing signals
- HD/ SD frame sync /delay (8 frames max)
- Audio delay, enabling Dolby-E processing delay correction
- Embedded audio gain adjustment for each video input
- Audio fade out/ fade in at switching or frame-wrap
- EDH processing

2 Specifications

Electrical SDI input

Number of inputs	2
Connectors	75 Ohm BNC
Equalization	Automatic; >300m @270Mbps w/Belden 8281, with BER < 10E-12 >130m @1485Mbps w/Belden 1694A, with BER < 10E-12
Input Return loss	>15dB, 5MHz -1.485GHz
Active input	
Input Return loss	>15dB, 5MHz -742.5MHz
passive bypass	>10dB, 742.5MHz - 1.485GHz
Jitter tolerance	SD limit: 10Hz-1kHz: >1 UI 10kHz – 5MHz: >0.2 UI HD limit: 10Hz-100kHz: >1 UI 100kHz–10MHz: >0.2 UI

Electrical Sync input

Connector	75 Ohm BNC
Format	Black & Burst, Tri-level
Input Return loss	>35dB @ < 10MHz, 30dB @ < 30MHz

Electrical SDI outputs

Number of outputs	4
Connectors	75 Ohm BNC
Return Loss O1, O2	>15dB, 5MHz -1.485GHz
Active output	
Output Return loss O1, O2	>15dB, 5MHz -742.5MHz
Passive bypass	>10dB, 742.5MHz - 1.485GHz
Return loss !O1, !O2	>15dB, 5MHz -742.5MHz >10dB, 742.5MHz - 1.485GHz
Output signal level	800mV +/- 10%
Output signal rise / fall time	SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var.
20% - 80%	HD limit: < 270ps, <100ps rise/fall var.
Amplitude overshoot	<10%
Output timing jitter	SD: <0.2 UI HD: <1 UI
Output alignment jitter	SD: <0.15 UI HD: <0.2 UI

Supported standards

SD, 270 Mbps	SMPTE 259M, SMPTE 272M-AC
HD, 1485 Mbps	SMPTE 292M, SMPTE 274M, SMPTE 291M, SMPTE 296M, SMPTE 299M
Video switch point definition and sync	SMPTE RP168 (tri-level), SMPTE 170m, ITU-R. BT.470
EDH	Compliant to SMPTE-RP165
Video Payload Identification	SMPTE 352M-2002

Power

Power consumption	3.5W @ 5V 1.2W @ 15V

3 Configuration

The board can be controlled manually via DIP switches, rotary switches and push buttons on the board, or through the graphical user interface provided by the system controller Multicon Gyda. Only the most frequently changed and/or most important settings are available on the DIP switches. If Multicon is used to do an initial setup of the other settings, these settings will be retained in the module for future sessions, even for manual mode.

3.1 Manual mode

To reach manual mode DIP16 labeled OVR on the board must be switched on (to the right) and the board must be re-booted. This takes the board out of Gyda control (if the switch was previously set to off) and over to DIP switch, rotary switch and push button control. This particular DIP switch (and the factory reset DIP switch) will only be read at start-up. Settings not controlled by any of these manual switches/buttons are kept unchanged from previous session (factory setup or Gyda setup).

The Manual Mode configuration controls are all found on the front side of the board. There are two sets of DIP switches, one rotary switch and two push buttons. The slide switch on the lower right side should be se to the lower position (“BP”) for all operation modes.

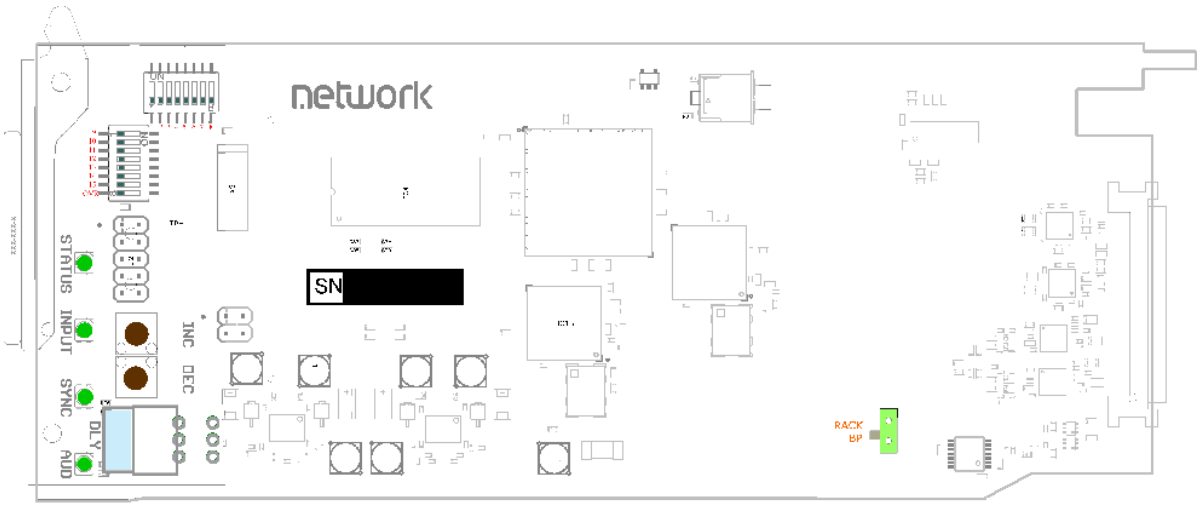


Figure 2: The figure shows a top view component printout of the board. LEDs, push-buttons, the rotary switch and the 2 sets of DIP-switches are colorized.

3.1.1 Rotary switch and push buttons

The *rotary switch*, labeled DLY, adjusts the *phase delay* by -5 to +4 video lines. It is only functional when a sync signal, black & burst or tri-level, is present at the sync input. The rotary switch is accessible from the board front.

The *push buttons,* labeled INC and DEC, are used to fine adjust the *phase delay* by samples. It can adjust within +/- ½ video lines for the present video standard.

These settings are part of the frame synchronizer, see chapter Frame synchronizer5.4 for further explanations.

3.1.2 Slide switch

The slide switch on the lower right side of the card switches between backplane sync input (BP) and Flashlink rack distributed sync (RACK) (Future feature upgrade of Flashlink frame). Switch moved down routes the backplane sync to the card.

3.1.3 Factory reset function

The factory reset puts the card back to its initial settings at delivery. These settings are just a start condition for the board, and new settings done by the user will still take effect and be stored.

The factory reset is done by setting DIP 15 and 16 to on and power up the card. The inputs should be removed. Then, pull out the card, put DIP 15 to off and power up the card again. The card will now reset. The board must be under power for at least 10 seconds for all the factory reset values to be stored for the next session.

3.1.4 DIP switch functions

The two sets of DIP switches are labeled with a number running from 1 to 15. The 16th DIP is labeled *OVR.*

> Note that the left DIP switch of the horizontal DIP package is number 1. The top DIP switch of the vertical DIP package is number 9.

Switch #	Function name	Function of DIPs	Comment
1-3	Frame delay	DIP[1 2 3] = [Off Off Off] => 0 frms DIP[1 2 3] = [Off Off On] => 1 frms DIP[1 2 3] = [Off On Off] => 2 frms DIP[1 2 3] = [Off On On] => 3 frms DIP[1 2 3] = [On Off Off] => 4 frms DIP[1 2 3] = [On Off On] => 5 frms DIP[1 2 3] = [On On Off] => 6 frms DIP[1 2 3] = [On On On] => 7 frms	With a sync-input present, this sets the minimum frames delay. Without a sync-input present, this sets the no. of frames delay relative to the input.
4-5	Lock & Hold time	DIP[5 6] = [Off Off] => Minimum DIP[5 6] = [Off On] => 1s DIP[5 6] = [On Off] => 4s DIP[5 6] = [On On] => Reserved	The time a signal must be registered before it is considered present (lock time), or the time it can be not registered before it is considered missing (hold time).
6	Audio gen	Off = 1kHz Sine On = Black sound	Fallback for embedded audio when input not present.
7	Emb. enable	Off: No audio embedded On: Audio embedded	When off, the audio is left un-touched on the SDI stream. When on, the audio configured to be embedded is embedded into the SDI.
8	GPIO setup	Off: SDI-CHO-2x1 mode On: FRS-HD-SDI mode	See the GPI input output description below.
9 - 11	Fade frames	DIP[9 10 11] = [Off Off Off] => 0 frms DIP[9 10 11] = [Off Off On] => 15 frms DIP[9 10 11] = [Off On Off] => 30 frms DIP[9 10 11] = [Off On On] => 45 frms DIP[9 10 11] = [On Off Off] => 60 frms DIP[9 10 11] = [On Off On] => 75 frms DIP[9 10 11] = [On On Off] => 90 frms DIP[9 10 11] = [On On On] => *** frms	The number of frames used to perform a fade-in or fade-out. The same value will be used for all four fade timers, all fading will be symmetrical. The value for Additional black frames will not be modified, i.e. the value from the previous Multicon GYDA controlled session will be preserved. The default is 0 frames. The special condition [On On On] will not modify the fade timers at all. This setting can be used to preserve asymmetric fade configurations from Multicon Gyda even in manual mode.
12	SDI OUT 1	Off: through mode On: processed mode	In through mode the video only goes through a re-clocker.
13	SDI OUT 2	Off: through mode On: processed mode	In through mode the video only goes through a re-clocker.
14	Video	Off: Color bar	This is the video generator signal

Switch #	Function name	Function of DIPs	Comment
	Generator	On: Black field	that is shown when input is considered missing, i.e. hold time has expired.
15	RESET	Off: Use values preset by GYDA. On: RESET to factory defaults	To reset, both DIP 15 and DIP16 must be set on before powering on. DIP 15 and 16 is read at power up. The reset is not done until DIP 15 is set back to off and re-powered.
16	OVR	Off: GYDA mode On: Manual mode	This DIP is only read at power up. OVR is short term for GYDA override

Table 1: DIP SWITCH FUNCTIONS

3.2 Gyda mode

All functions of the card can be controlled through the Gyda control system. The Gyda has an information page and a configuration page.

3.2.1 Information page

The information page shows a dynamic block-diagram of the board and some additional information text. The block diagram updates with the boards status, showing input signal selected, signals missing (by red crosses over signal lines) and routing through switches.

The text on the information page gives additional information or information about functionality not displayed on the dynamic block diagram.

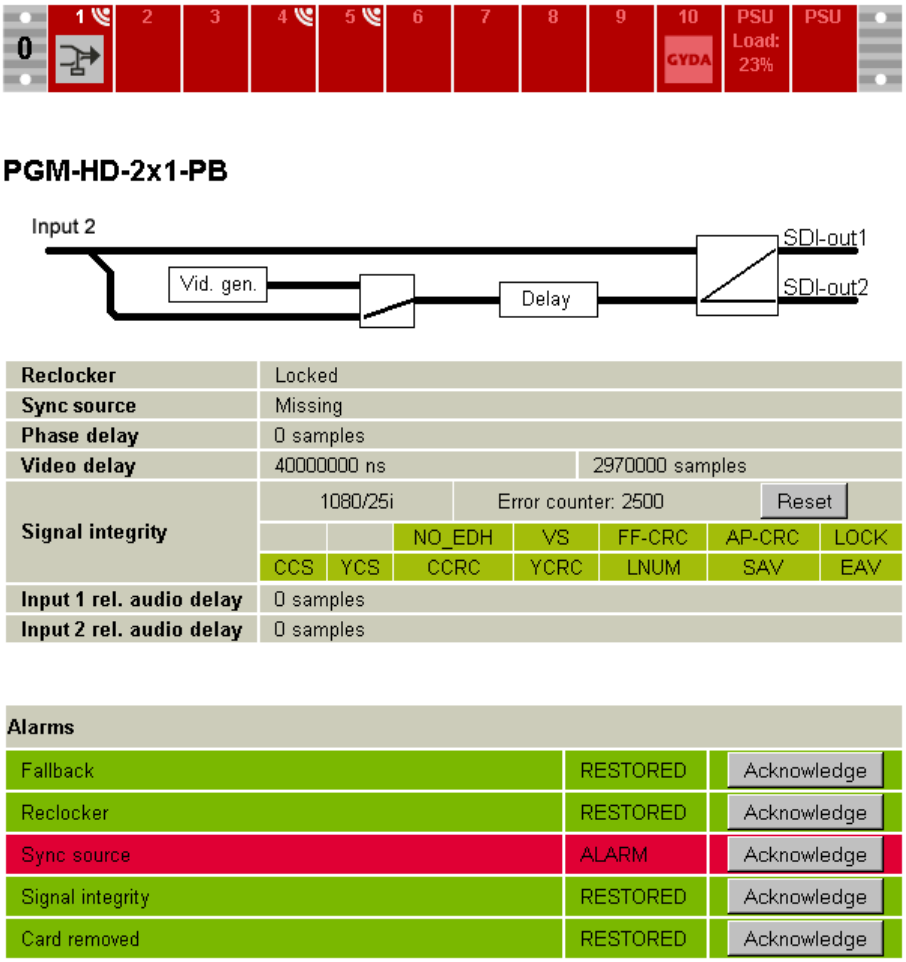


Figure 3: Gyda information page

The *Reclocker* block shows if the card is currently locked to an input. Possible values are *Locked* or *Loss of lock*.

The *Sync source* block shows if a valid sync signal is detected on the dedicated sync input, or if output video is generated with the SDI input as the input as the only frequency reference. Possible values are *Black&Burst*, *Tri-level*, *SDI*, and *Missing* (when no input of any kind is present).

The *Phase delay* block shows the currently used phase delay, re-calculated to video samples for the current video standard.

The *video delay* block shows the actual delay used between input and output video, re-calculated to both nanoseconds and to video samples for the current video standard. Note that although there could be rounding errors in these re-calculations, the delays will still be exactly as set by the user in the configuration page.

The *Signal integrity* block shows the current input video standard and a counter of frames seen with errors. The counter can be reset, but will also restart when it reaches 2^{16} = 65536 errors. The list of error bits shows a snap-shot of the last frame reported to Multicon, and errors are indicated with a red background color. This is based on the raw error data; If the user has selected to mask off certain errors, these errors will still be shown here in the snap-shot, but they will not cause the counter to be increased.

The two *relative audio delay* blocks show how much embedded audio will de delayed relative to the video, in 48 kHz audio samples. This delay can be different for the two video inputs.

3.2.2 Configuration page

The different configuration possibilities are explained in detail in Chapter 5, under the corresponding functions.

3.3 Connections

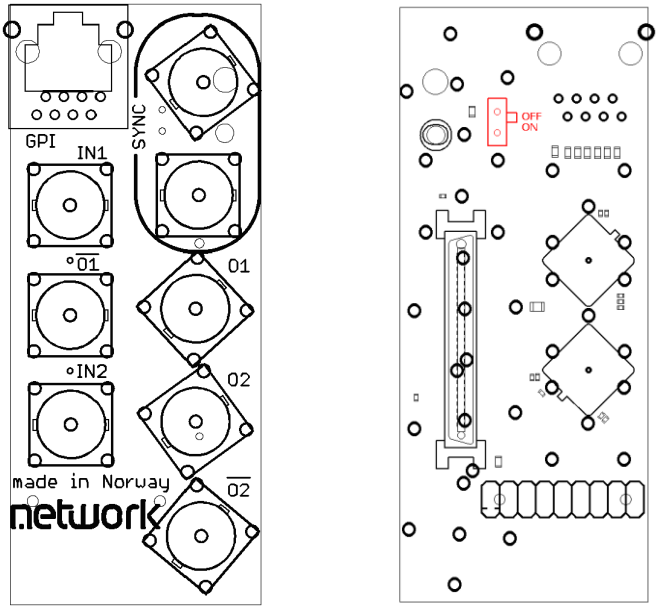


Figure 4: PGM-HD-2x1-PB backplane
right: connection side left: component side

The backplane for the PGM-HD-2X1-PB is also labeled PGM-HD-2x1-PB. The table below shows the connectors and their functions.

Function	Label	Connector type
HD/SD-SDI input 1	IN1	BNC
HD/SD-SDI input 2	IN2	BNC
HD/SD-SDI output 1	O1	BNC
HD/SD-SDI output 1 inverted	$\overline{O1}$	BNC
HD/SD-SDI output 2	O2	BNC
HD/SD-SDI output 2 inverted	$\overline{O2}$	BNC
Black & Burst/ tri-level input	SYNC	BNC
Black & Burst/ tri-level input	SYNC	BNC
GPI in	GPI	TP45, pin 5 & 6
GPI out	GPI	TP45 pin 1, 2, 3, 4, 7 (pin 8 = GND)

Table 2: Connector functions

Unused SDI inputs/outputs should be terminated with 75 Ohm.

3.4 Sync input

The two sync inputs on the backplane are internally connected together. It is possible to use one as input and the other as a looped output. The backplane also features a switchable termination. By setting the red switch in Figure 4 to “on” (the lower position) the sync input will be terminated with 75 Ohms.

4 Operation

4.1 Front panel LED indicators

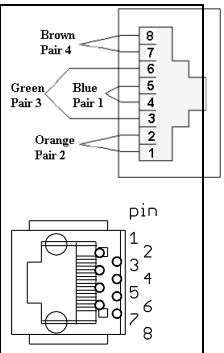
Diode \ state	Red LED	Orange LED	Green LED	No light
Card status	PTC fuse has been triggered or FPGA programming has failed	Module has not been programmed, RESET and OVR DIPs are on, or module is updating firmware.	Module is OK	Module has no power
SDI input status	Video signal absent.	Video signal present but card not able to lock VCXO	Video input signal in lock	Module has not been programmed
Sync input status	Sync signal absent	Sync signal present but card unable to lock VCXO	B&B or Tri-level sync in lock	Module has not been programmed
Audio input status	No audio embedded in incoming video	One, two or three audio groups embedded in incoming video	4 audio groups embedded in incoming video	Module has not been programmed

4.2 GPI alarms

The GPI alarms of the PGM-HD-2X1-PB are fully compatible with the HD-SDI-CHO-2x1 module, and thereby also the “change-over mode” of the FRS-HD-CHO (FRS-HD-CHO can also be configured to be compatible with the FRS-HD-DMUX module). See the table in the next sub-chapter for a detailed description.

4.2.1 Functions of 8pin modular jack

GPI name	Function	Pin #	Mode	Direction
Status	General error status for the module.	Pin 1	Inverted Open Collector (open is alarm)	Output
LOS[1]	Loss of signal or lock at selected input	Pin 2	Open Collector	Output
Input 1 selected	Input 1 selected (IN1)	Pin 3	Open Collector	Output
Input 2 selected	Input 2 selected (IN2)	Pin 4	Open Collector	Output
Select input 1	Fade in input 1, after fade out of input 2. Activating simultaneously as pin 6 will give fade to black.	Pin 5	TTL, 0V = active level	Input
Select input 2	Fade in input 2, after fade out of input 1. Activating simultaneously as pin 5 will give fade to black.	Pin 6	TTL, 0V = active level	Input
Input 2 selected	Connected to pin 4 on backplane	Pin 7	Open Collector	output
Ground	0 volt pin	Pin 8	0V.	



[1] EDH errors will not be shown at GPI output.

5 Functional description

The goal of this chapter is to give an overview of the data path for audio and video, show which processing options are available and link this to the user interface in Multicon Gyda.

5.1 An overview of the data path

HD/SD-SDI input is selected from input 1 or 2, equalized, re-clocked and transferred to a processing unit. Here the signal is first sent through a *de-glitcher* that cleans up errors that might appear on input signal, e.g. from switching. After the de-glitcher the parallel video is split in two paths, one going directly to a *frame-store buffer*, the other sent to the *audio de-embedder*.

The 16 audio channels coming from the de-embedder are bundled **in pairs** and sent to an audio store buffer (being the same as the frame store buffer). The audio is fetched from the audio store buffer according to a user specified delay (can be different for each of the two video inputs) and sent to the A*udio Processing Block*, where the paired channels may have gain adjusted (also specific for each of the video inputs). After the audio processing block the audio enters the *Audio Embedder* to be re-embedded.

The video (with audio still inserted) is fetched from the frame buffer with the user specified delay and sent to a *Video processing block* (which performs the video fading), followed by an *EDH processing block*. After the EDH block the video and audio is embedded according to the user settings and the video is sent from the processing unit to a re-clocker. Here the signal is converted back to SDI and sent to a 2x2 buffered output switch.

The output switch is a 2x2 cross point selecting between a signal which has only been equalized and re-clocked (“Through”) and a signal which has been fully processed (“Processed”). The two output signals are each sent to two paired (non-inverting and inverting) outputs.

5.2 Video input selection and fading

The PGM-HD-2X1-PB has two equivalent electrical inputs. The active input can be selected directly from the graphical user interface, or input control can be handed over to the GPI input lines. 5 configurable delays are used to control how the fading between the two physical inputs appear. The “fade in” settings control how many video frames will be used to go from “black” to “full luminosity”, while the “fade out” settings control how many video frames will be used to go from “full luminosity” to “black”. A user specified number of black frames can also be inserted between the “fade out” and the “fade in”.

When an input is selected, for instance “Fade to 1”, the actions performed will depend on the current state of the module. If the module already has input 1 selected, no actions will be performed. If the module has been forced to black, input 1 will immediately start to fade in according the “Input 1 fade in” setting (see below). If the has input 2 selected, output 2 will immediately start to fade out according to the “Input 2 fade out” setting. Once the fade out is completed, a number of additional black frames will be inserted according to the “Additional black frames” setting. Then the fade in of input 1 will finally commence according to the setting in “Input 1 fade in”.

When selecting “Fade to 2”, the explanation above still holds if “1” is substituted for “2” and vice versa.

If “Fade to black” is selected, no actions will be performed if the module is already set to black. If one of the physical inputs has been selected, the video will fade to black according to “Input 1 fade out” or “Input 2 fade out” respectively, and then stay black

until one of the physical inputs is selected again. This is also true when input select is controlled from the GPI inputs. Two GPI input lines are available and activating one of them will select the corresponding physical input, while activating both of them at the same time will force a fade to black. The video will then consist of black frames only until a single line is activated again. If both lines are released at exactly the same time, the module continues to output black frames. If – say – line 1 is released first, while line 2 stays activated, that will be interpreted in the same way as if line 2 was activated from the released position, and a fade to input 2 will be performed.

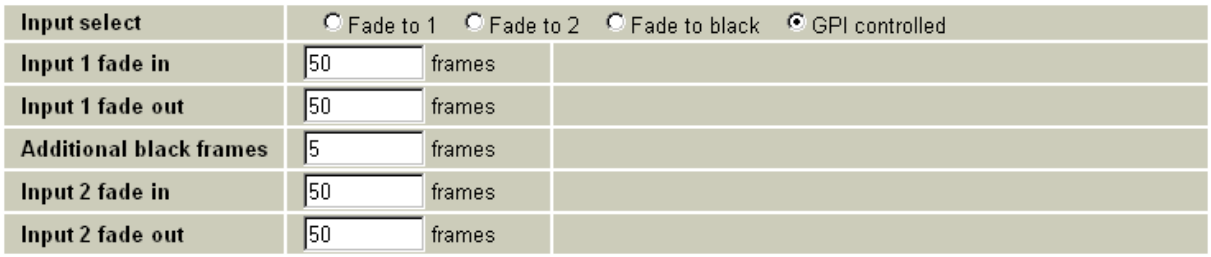


Figure 5: Gyda view of input select with additional control blocks.

> Note that if a new fade/switch command is issued while the previous one is still being executed, the first fade will be abrupted and the second one will be started immediately. This happens regardless of how the command was given (Multicon or GPI). Continuous toggling of one of the GPI lines will constantly restart the fade out action and thereby returning the luma gain to 1, and the result will be perceived as flickering in the video luminosity.

5.3 De-glitcher (no settings)

The de-glitcher corrects timing errors within a line. The de-glitcher has a 2048 samples buffer. When the first signal is present, we call it the “initial phase signal”, data is taken from the centre of this buffer. If the timing reference of the video signal changes, when for instance a new source being switched into the signal path, the timing errors occurring by this change will be corrected if the new timing reference is within +/-1024 samples of the “initial phase signal”. This also goes for all consecutive timing references.

If a signal is more than +/-1024 samples off relative to the “initial phase signal”, the output will repeat the last frame, refill the 2048 samples buffer and take out data from the centre of the buffer. This new signal is now considered the “initial phase signal”. Audio will fade out when a frame repeat is being done, and fade in at the new frame.

Hence, it produces an error free video output without frame wrapping when the video input comes from a router with synchronous input video signals that all lies within +/-1024 samples of each other.

> The de-glitcher output is always seamless. When a signal is repeated the audio is faded out. It fades in at the new frame.

5.4 Frame synchronizer

The frame synchronizer consists of a frame store buffer and some control logic. The frame store buffer can store up to 8 full HD frames. Data is fetched from this buffer according to the user settings by force of the control logic. The control logic sets the frame synchronizer into different modes dependent on the presence of a sync input.

5.4.1 Frame sync mode

If a sync input (B&B or Tri-level) is present, the frame synchronizer will output a signal that has a delay relative to this signal. Two parameters can be set; "**Phase delay**" and "**Video delay**".

Phase delay	0	lines	0	samples	
Video delay	2	frames	0	lines	0 samples

Figure 6: Gyda view of the video delay settings

Let us first focus on the *phase delay*, which also may be called “output phase delay”. This parameter can be positive or negative, and determines the relationship between the outgoing video and the sync signal. The parameter really determines a delay on an internal sync signal, isync[2]. The output is synchronous with isync, see Figure 7.

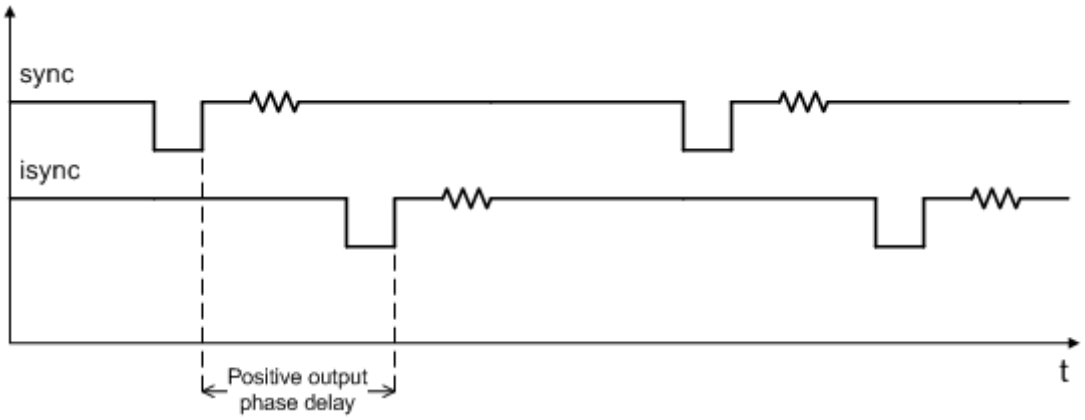


Figure 7: Positive phase delay

Figure 7 show how the sync signal and the isync signal would look on an oscilloscope, if converted to analogue signals. The delay of isync can be given in frames, lines, and samples. The delay can be negative, see Figure 8.

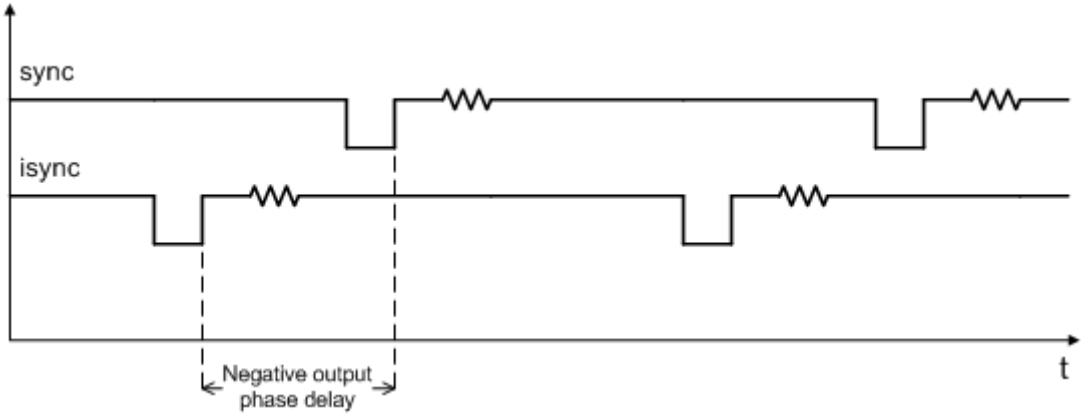


Figure 8: Negative phase delay

The *phase delay* can thus be written in several ways, a large positive delay will equal a small negative delay, because there is wrap-around on a frame basis. It follows that it is not useful to specify a *phase delay* larger than 1 frame. Strictly speaking the range could have been limited to -1/2 frame to 1/2 frame. For convenience, the delay range is allowed to be from -1 frame + 1100 samples to 1 frame – 1100 samples.

[2] Note that *isync* is not a physical entity, but a term used in this context to explain the delay process and the use of the configurable parameters related to this process.

In order for FRS-HD-DMUX to honor the *phase delay* setting, it should ideally delay the incoming video between 0 to 1 frames. Because the processing delay through the card is 2 lines minimum, the actual window is between 2 lines and 1 frame + 2 lines. Hence, with the parameter (minimum) *video delay* set to 2 lines (the least number possible for the parameter); the output video will be between 2 lines and 1 frame + 2 lines delayed, with respect to the incoming video. A common occurrence in practical use is to synchronize an incoming video with a sync, but to let the outgoing video lead some samples or lines to the sync. This can easily be accomplished. Say that we want the outgoing video to occur 50 samples before the sync. We will then set the *phase delay* to -50 samples, and the *video delay* parameter to 2 lines. For convenience, let us assume that the incoming video is iso-synchronous, but that it lags 20 lines after the sync. We will then have the situation shown in Figure 9.

Note that the numbers in circles in the next figures are visualizing the video frames.

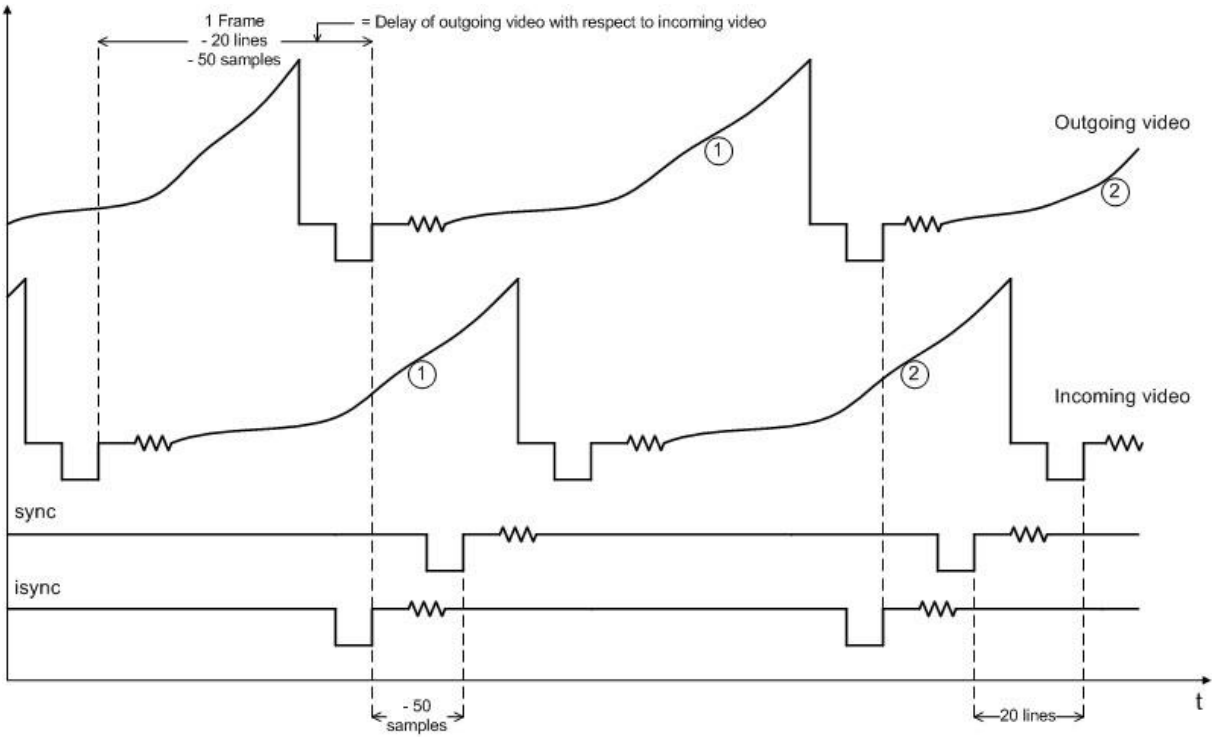


Figure 9: Example of delayed outgoing video

To match larger processing delays, one will want to first delay the incoming video, and then synchronize the video. This is equivalent to introducing a delay line for the incoming video, and then synchronizing the output of the delay line with sync. In effect, one moves the delay-window start; this is equivalent with setting the *video delay* to a larger value.

Let us assume that the *video delay* is set to 2 frames, 200 lines. In that case the outgoing video will be between 2 frames + 200 lines and 3 frames + 200 lines delayed with respect to the incoming video. For convenience, let us assume that the incoming video is iso-synchronous, but that it lags 25 lines after the sync. Let us also assume that the *phase delay* is set to -60 samples. We will then have the situation shown in Figure 10.

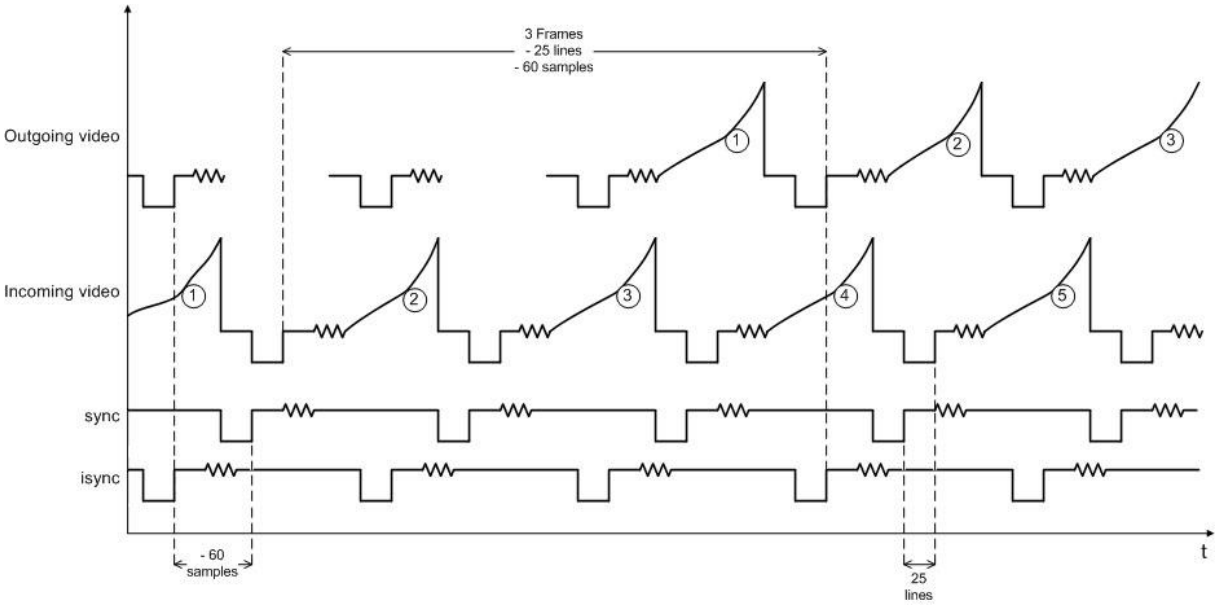


Figure 10: Another example of delayed outgoing video

To reiterate: The *phase delay* can be both positive and negative and sets the difference between the phase of the sync input and the video output. The *video delay* sets the delay between video output and video input. However, the actual delay might be longer as it also needs to phase up to the sync input. The actual delay may be up to 1 frame longer than the minimum video delay.

> The user may specify a *video delay* between 2 lines (min) and 7 frames (max).

The two parameters allow a user to delay the incoming video, and reference it to the sync input. By this mechanism, the user can precompensate processing delay in other equipment. The *video delay* setting simply determines a lower limit to a 1 frame wide window into a long delay line. The *phase delay* may be seen as a specification of the delay between the sync input, and a signal "isync". The output video is always synchronized to isync. A few more examples:

Example 1: The SDI input signal is isosynchronous to a sync signal, but 12 lines, 0 samples delayed. The *video delay* is set to 1 frame, 0 lines and 0 samples. The *phase delay* is set to 65 samples. The actual delay between the input video and the output video will be 2 frames - 12 lines + 65 samples.

Example 2: The SDI input signal is asynchronous to the sync signal (the frame frequency is slightly different). The *video delay* is set to 1 frame, 13 lines and 0 samples. The *phase delay* is set to -1 line. The actual delay will gradually change between 1 frame and 13 lines to 2 frames and 13 lines. The output will appear 1 line (in the output video format) ahead of the sync signal.

Example 3: The SDI input signal is isosynchronous to the sync signal, but 12 lines ahead of the sync signal. The *video delay* is set to 1 frame, 0 lines and 0 samples. The *phase delay* is set to -2 lines. The actual delay between the input video and the output video will be 1 frame + 10 lines.

The frames and lines are measured in units of the output SDI video standard. If the output SDI standard is 1080i25, a delay of one line is equal to 35.5us. If the output SDI standard is 720p50, a delay of one line is equal to 26.6us. If the output SDI standard is 625i25, a delay of one line is equal to 64us.

For a scenario where the card receives different HD video standards, (e.g. 1080i25 and 720p50) the user may want to conserve a specific delay in microseconds for all HD video standards. This is accomplished by specifying the delay in number of samples instead of frames and lines. (For HD video standards the sample frequency is equal over standards, but the line and frame frequencies are different for the different standards).

If video input disappears

Given that stable SDI input and sync input exists: If the SDI input disappears, the picture will freeze for <*hold time*> and then go to video generator if the card is in default configuration. When the SDI input disappears, the Frame Delay pulses at the back plane will also disappear.

If video input reappears

Given stable sync input, the video will reappear after <*lock time*> of locked video input if card is in default settings.

If sync input disappears

Given that stable SDI input and sync input exists: If the sync signal disappears, the card will act as in frame delay mode, see Chapter 5.4.2.

NOTE: This will result in a frame roll as the delay changes.

If sync input reappears

Given that a stable SDI input exists: If the sync signal reappears the delay mode will change back to Frame Sync mode. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

If both signals disappears

The picture will first freeze for <*hold time*> and then go to video generator. The output is now referenced to the local clock source. However this clock source will be kept within 1 ppm of the last sync source.

5.4.2 Frame delay mode

In this mode a sync signal is not present. The delay set is then directly related to the incoming video. 1 frame and 1 line delay, means that the output will be 1 frame and 1 line delayed version of the input.

If video signal disappears

The picture will first freeze <*hold time*> and then go to video generator. The output is now referenced to the local clock source. However this clock source will be kept within 1 ppm of the last video source.

If video signal reappears

If the input video signal reappears, the video will reappear on the output <*lock time*> after stable input video. The delay will be set to the same delay as before loosing input.

NOTE: This may cause a frame roll.

If a sync input appears

Given that a stable SDI input exists: If a sync signal appears the delay mode will change to Frame Sync mode, see Chapter 5.4.1. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

5.5 Fallback to video generator

The video generator can produce several simple signals: Colorbar, Colorbar with a moving box, Check field, and Flat field.

The Flat field can be set up to produce any 10bit (0-1023) luma and chroma value, or to produce a predefined color.

For this module the video generator can only be used as a fallback, i.e. when the selected video input disappears. When the input goes missing the picture will freeze, and if the input reappears during this time, the freeze condition will be lifted without the generator being used. If the signal hasn't returned within approximately 1000 milliseconds, the generator will be switched in. Once the generator has been switched in, the input will have to be present and stable for approximately 1000 ms before the module will switch back from the generator.

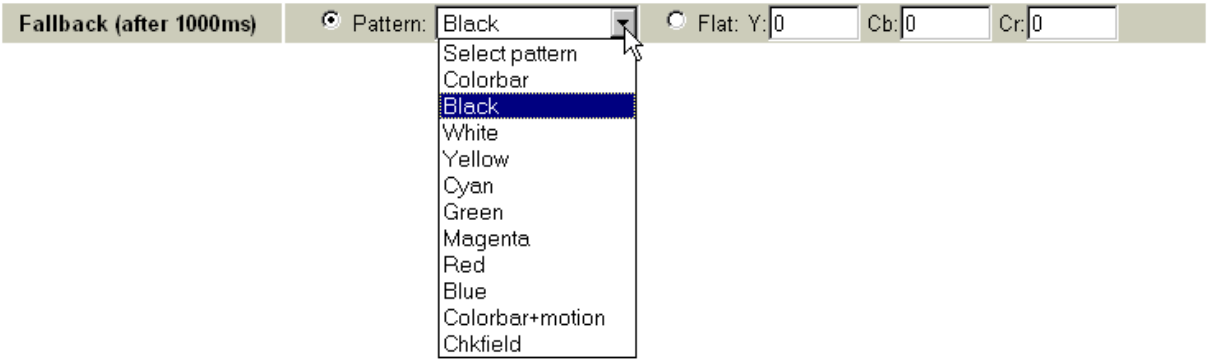


Figure 11: Gyda view of the video generator

5.6 On-screen label generator

The label generator consists of 2 lines, 16 characters each. Two different sizes can be selected, in addition to black text with white border or white text with black border.

The intended main function of this generator is to enable the user to automatically superimpose a text label to the internal generator at loss of input signal. This is done by selecting the "Auto" tick-box on the "Label generator" block in the Multicon GYDA configuration page. In a long chain of cards, this can be a very way to identify where the signal was actually broken and replaced with a generated output.

It is also possible to always superimpose the label on the incoming SDI by ticking the "On" box.

> Note that to see the label on an output the video output selection must be set to "processed" for this specific output.

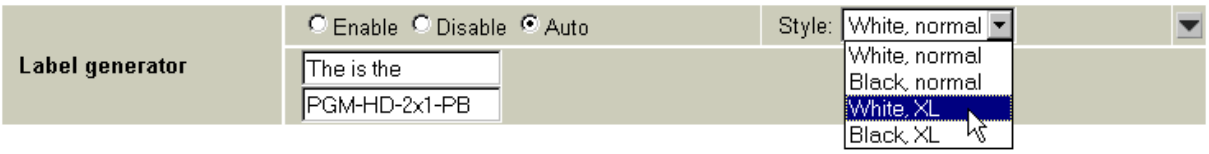


Figure 12: Gyda view of the label generator

5.7 Video monitor

The incoming video is analyzed and the number of frames with errors are counted. Individual errors (or types of error) can also be ignored. The errors available for selection in this module are:

EAV: End of Active Video error

SAV: Start of Active Video error
LNUM: Line numbering error (HD only)
YCRC: Luma CRC error (HD only)
CCRC: Chroma CRC error (HD only)
YCS: Luma checksum error
CCS: Chroma checksum error
LOCK: Lock error, i.e. reclocker unlocked
AP-CRC: Active Picture CRC invalid
FF-CRC: Full-Frame CRC invalid
VS: Video Standard error, i.e. reclocker locked but unrecognized video standard
NO_EDH: No EDH package (SD only)

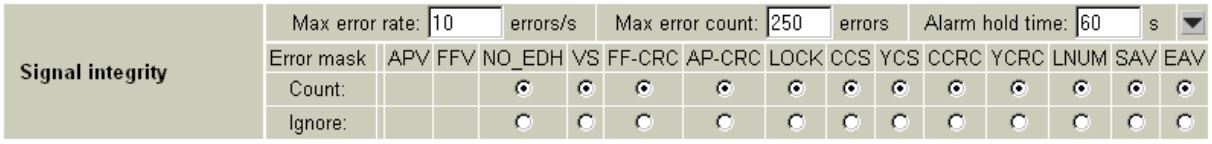


Figure 13: The video monitor and error counter.

5.8 Video payload legalizer (no settings)

This module has the SDI legalizer permanently enabled. The legalizer hard clips the upper and lower limit of the video payload to the following limits:

Upper limit	Luma:	3ACh
	Chroma:	3C0h
Lower limit	Luma:	040h
	Chroma:	040h

5.9 EDH processing block (no settings)

This module has the EDH processing block permanently enabled. The EDH processing block extracts the EDH package from the video, updates the EDH flags according to SMPTE RP165 and inserts the EDH package into the ancillary data of the video.

5.10 Video output selection

The board has four SDI outputs in total, but they form two pairs where each consists of one inverted and one non-inverted BNC output (see Table 2: Connector functions on page 10). The routing is controlled per pair.

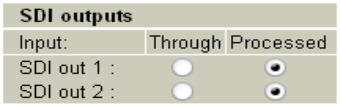


Figure 14: Gyda view of SDI output selection block

When processed is selected, it is possible to either output video generator or mute the output. This is done at the *video in - mode* by selecting *Video gen.* or *Mute*. This will not have any effect on outputs set in through mode.

5.11 Audio de-embedder and embedder (no settings)

The Audio de-embedder extracts all audio embedded in the video stream. The de-embedder is always enabled, and for this module the embedder is also permanently enabled, otherwise it would not be possible to fade audio with the video.

5.12 Relative audio delay

An audio delay relative to the video output can be specified commonly for all de-embedded channels. This is done from Multicon Gyda. The audio delay is specified in audio samples relative to the output video, and can be both positive and negative. For this module *two different* relative audio delay scan be specified, one for each video input. This enables the user to correct for different audio/video alignments for the two sources.

> Note that as the audio delay is relative to the video output it is possible to specify an audio delay that will be an actual negative delay. This will cause audio errors.

If using a negative relative audio delay, the positive *video delay* (see chapter 5.4 Frame synchronizer) needs to be set higher than the wanted negative relative audio delay. In Figure 15 below the audio is given a negative delay when video input 1 is selected. Assuming a video format with 50 frames/second, the -960 samples would correspond to -1 frame[3].

Figure 15: Relative audio delays.

Dolby-E and delay handling

The PGM-HD-2X1-PB can re-align Dolby-E with video (Dolby-E processing equipment typically causes one frame delay for the audio, which can be compensated with a relative audio delay of -1 frame as above). The module does however ***not*** decode/re-encode Dolby-E.

5.13 Audio processing

The audio level of the embedded audio can be adjusted. This can either be done to match the level of the two video inputs, or to match a third level or standard. The gain entered will be applied to all embedded audio channels for that respective video input.

Figure 16: Embedded audio processing.

> Note that the “Mode” selections have no effect. These drop-down menus will be removed from the user interface before the final release of the product.

Audio gain and fading

Audio gain is a 16 bit value that can be set for each stereo pair going into the audio processing block. The actual gain is the 16 bit value/100 dB. The gain range is set to [-96 dB, +96 dB] with a gain step of 0.1 dB. Audio fading is handled as an additional term in dB (which would translate to a multiplication factor in linear sample space), the size of which depends of the current position in the fade-in or fade-out cycle. The sum of the fixed gain setting and the time-variable gain from fading is what is limited to [-96 dB, +96 dB]. What this means is that if audio gain is set to -A dB to begin with, there will be a (96-A) dB range available to do the actual fading. The gain will always bottom out at -96 dB. Setting the gain higher than 0.0 dB will have no similar adverse effect.

[3] To calculate number of audio samples/frame simply divide 48000 with frame rate (24Hz, 25Hz, 29.97Hz, 30Hz, 50Hz, 59.94Hz or 60Hz)

Note that non-audio data is ignored and left unchanged by the audio gain function. This includes Dolby-E, which will not be gain adjusted (or faded) by this module. To do that would require a full decode/re-encode of the Dolby-E data.

6 RS422 commands

6.1 FLP4.0 required commands

Block	Blk #	Commands	Example	Response	Control
-	-	?	?	*product name*\ SW rev *n.m*\ FW rev *r.s*\ protocol ver 4.0\	***Hello* command**. *Note 1: No other commands will be available until the card has received this hello.* *Note 2: This command will also enable checksums.* *Note 3: Cards are designed to be hot-swappable. To sync with the start of a new command, the cards will wait for a <lf> character before looking for a valid command.*
conf	0	-	conf 0	*too long to list*	**Configuration settings** Retrieves the card's configurable settings. Each addressable block is represented by a single line. Dynamic status *may* be included in response, but is usually reported in *info* only.
-	-	info	info	*too long to list*	**Dynamic status info** Blocks with static settings only will usually not be included, see *conf* above.
-	-	chk off	chk off	ok	**Checksum off** If issued twice in succession, this command will disable checksums. Note: Responses will still have the checksums appended. *NOTE1: ? command turns the checksum back on*
-	-	locate on <seconds> locate off	locate on 3 locate off	ok	**Card locator** This command will cause all the LEDs to flash for a user specified number of seconds. If omitted, the value <seconds> will be set to a default of 120 seconds. The flashing can be terminated at any time with *locate off*.
-	-	address	address	address <address>	**Card address** This command will check and update the card's current rack and slot address, which is normally only done at start-up.
-	-	filename	filename frshdpgm-0-105.ffw filename frshdpgm-0-100.mfw	<name>'.'<extension>	**Firmware upgrades** The <name> part must match the card's hardware and include a revision number, and the extension must be either 'ffw' for FPGA firmware or 'mfw' for microcontroller firmware. After running this command the board will wait for the firmware in Intel-hex format.
-	-	fin	fin	ok	**Finalize** Finalize the programming of the microcontroller. See description of the uC bootloader (separate document).

misc	0	-	NOT AVAILABLE BY COMMAND. ONLY FOUND in Conf 0	prog | fin ' ' | ovr	**Misc info** *prog* if the card is freshly programmed by the bootloader and the program is still un-finalized. *fin* is the normal condition. *ovr* if DIP-switch 16 is set to the ON position and the card is under DIP-switch control. Note 1: The info part of misc has additional functionality when locate is used: *locating <remaining seconds>*. This enables a visible countdown clock in Gyda, but is not a required part of FLP400.

6.2 Normal control blocks

Block	Blk #	Commands	Example	Response	Control
aprc	0-17	lvl <gain>	aprc 7 lvl -400		**Audio processing** 'lvl' means level and is the gain setting. aprc 0 and 1 are related to input 1 and 2. aprc 2-9 can be used to set gain for individual channel pairs of input 1, while aprc 10-17 can be used to set gain for individual channel pairs for input 2.
ceq	0	-	ceq 0	cd | ncd	cable equalizer for electrical input 1. No control, only used to report *carry detect* or *not carry detect.*
ceq	1	-	ceq 0	cd | ncd	cable equalizer for electrical input 2. No control, only used to report *carry detect* or *not carry detect.*
cho	0-1				No commands available. Included to show internal status and to update Gyda graphics.
dly	0	<frames>frms	dly 0 2frms	'tgt' <frames> frms	**Video delay** This sets the minimum video delay of the card. In info this block reports back the current delay in nanoseconds. This will vary with the incoming video standard.
dly	1-5	<frames>frms	dly 3 4 frms	'tgt' <frames> frms	**Fade controls** dly 1: input 1 fade-in time dly 2: input 2 fade-out time dly 3: additional black frames dly 4: input 2 fade-in time dly 5: input 2 fade-out time
dly	6-7	<audio_samples>sps	dly 6 30sps dly 7 -960sps	'tgt' <audio_samples> sps	**audio delay** The audio delay is given in audio samples. Audio delay is always given relative to video.
dly	8	<lines>lines <samples>sps	dly 8 1lines -30sps	'phase' <lines> lines <samples> sps	**Video phase** If lines != 0 the resulting phase will vary with incoming video standard, see dly 0 above.
gpi	0	act | inact	gpi 0 act gpi 0 inact		**EDH generator** This gpi works as a simple 2:1 switch. inact : EDH gen. off act : EDH gen. on
mtx	0	<i1> <o1> ...<iN> <oN> <i1> <o1>,<o2>,...<oN>	mtx 0 0 2 1 4 5 5 mtx 0 0 0, 1 1, 2 2 mtx 0 0 0-9	size M:N i1 i2 i3... iN	**Audio matrix** mtx 0 (size 10:8) controls the audio matrix; outputs 0-7 are embedded sound; inputs 0-7 are de-embedded audio,

		<i1> <o1> - <o2> ..or the above combined	mtx 0 0 0 1 1 2 2-7		8=1kHz sine, 9=Black/silence *Note: Any combination of the three basic commands are allowed, for instance the following command to set up a 10x10 audio matrix in a single line:* *mtx 0 1 1 2 2 3 0,3-7* *=> mtx 0 size 10:10 3 1 2 3 3 3 3 3 3*
mtx	1	<i1> <o1> ...<i2> <o2> <i1> <o1>,<o2>	mtx 1 0 0 1 1 mtx 1 0 0,1	size M:N i1 i2 i3... iN	**Video output matrix** mtx 1 (size 2:2) controls the video output switches. 0: Through mode (re-clocked only) 1: Processed mode (SDI from FPGA
mtx	2	<i1> <o1>	mtx 2 0 0 mtx 2 1 0	size M:N i1 i2 i3... iN	**Audio embedder bypass** 0: Embedding disabled 1: Embedding enabled
mtx	3	<i1> <o1>	mtx 3 0 0 mtx 3 2 0	size M:N i1 i2 i3... iN	**Video input select** 0: (Fade to) input 1 1: (Fade to) input 2 2: (Fade to) black 3: GPI controlled
rcl	0	-	rcl 0	lock | lol	**Reclocker** No control available. Only used to report *lock status.*
sync	0	-	sync 0	'lol' | ('lock' ('trilvl' | 'bb' | 'sdi'))	Frequency reference for video output. Status only, no commands available.
vgen	0	cbar | chkfield | white | yellow | cyan | green | magenta | red | blue | black flat <Y> <Cb> <Cr> video <lns>/<rate><scan> wss (auto|off | (on <wss_val>))	vgen 0 cbar vgen 0 flat 200 0 100 vgen 0 video 1080/24p vgen 0 video 1080/25p vgen 0 video 1080/25i vgen 0 video 1080/29i vgen 0 video 1080/30i vgen 0 video 720/24p vgen 0 video 720/25p vgen 0 video 720/29p vgen 0 video 720/30p vgen 0 wss auto vgen 0 wss on 7	video <lns>/<rate><scan> wss (auto| off | (on <wss_value>)) (cbar | chkfield | white | yellow | cyan | green | magenta | red | blue | black | (flat <Y> <Cb> <Cr>))	**Internal video generator.** The video generator will be activated in two different ways: If selected as a fallback option the generator will generate the selected pattern when the other input(s) are missing, and then use the video settings from the last external source present. It can also be selected as the main input in cho 1, in which case its own video settings will also be used.
vmon	0	msk <24b_mask> reset	vmon 0 msk 0x0E0A vmon 0 reset	msk <24b_mask>	**Error detection and handling** Error counting. The count itself is reported in info. Errors can be masked off and not counted; this is the purpose of the mask. The counter itself is 16b and will wrap around, but can also be reset by issuing *reset*.
vprc	0	lglz on | lglz off (y | cb | cr) <gain> <offset>	vprc 0 lglz on vprc 0 lglz off vprc 0 y 8192 0 vprc 0 cb 2000 0 vprc 0 cr 1000 1000		**Video processing block** Gain and offset are both signed fixed point numbers. Gain is in 2.13-format, while offset for Y and the chroma channels are given in 10.2 and 9.2 respectively.

					Gain range is 0 – 32767, $Gain_{=0x}$ = 0, $Gain_{=1x}$ = 8192, $Gain_{=4x}$ = 32767 Luma Offset range is -4095 – 4095, $Offset_{=0}$ = 0 Chroma Offset range is -2047 – 2047, $Offset_{=0}$ = 0

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
   - Operating room temperature range: 0°C to 45°C
   - Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:
   - Temperature range: -10°C to 55°C
   - Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the “Administrative Measure on the Control of Pollution by Electronic Information Products”. In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

組成名稱 Part Name	Toxic or hazardous substances and elements					
	鉛 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
PGM-HD-2x1-PB	O	O	O	O	O	O
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006. X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.						

This is indicated by the product marking:

A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site http://www.nevion.com/. Please contact Nevion’s Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.