FSR-HD

HD-SDI Frame Synchronizer with Audio De-Embedding

User manual

Rev. G

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Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
G	F	2015-01-21	AJM	Changed text in Chapter 2. Updated logo.
F	5	2012-12-04	JD	Changed HD sensitivity
5	4	2012-08-10	TB/JD	Added information on audio min/max delay. Updated template
4	3	2008-12-15	NBS	Rewritten Chapter 3.5.1. Changed text in Chapters 1, 3 and 4. Corrected Chapter 3.7.1.
3	2	2008-11-12	SHH	Added information about termination of loop-thru on rev.1 backplanes. Added drawing and description of termination on rev.2 backplane
2	1	2008-10-21	NBS	Corrected information about FACTORY reset.
1	0	2008-06-11	SHH / AS	Changed name on manual from FRS-HD-DMUX to FRS-HD. Change in functionality description: Page 15: the remark that push button settings are reset at power down was removed as this setting is stored by the microcontroller.
0	-	2008-03-17	SHH	Initial release.

Contents

1 Product overview

Figure 1: Simplified block diagram of the FRS-HD-DMUX card

The Flashlink FRS-HD-DMUX synchronizes a HD-SDI or a SD-SDI input to a reference. The reference can be a traditional black & burst signal or tri-level sync. The HD-SDI/SD-SDI output can be adjusted relative to the sync signal. The FRS-HD-DMUX also has a de-glitcher to give error-free synchronous switching.

FRS-HD-DMUX can be used as a frame delay. The adjustable delay is then relative to the input SDI signal.

The audio embedded on the SDI is de-embedded and can be delayed relative to the video. Each audio stereo pair can be swapped through a matrix before they are embedded back to the SDI. It is also possible to disable the embedder function and keep the SDI stream unaltered.

The user parameters of the card can either be changed by switches on the board, or by the control interface GYDA.

1.1 Product versions

FRS-HD-SDI   SD/HD frame sync with internal audio handling and GPI I/O control, 4 SDI outputs

FRS-HD-DMUX   SD/HD frame sync, analogue stereo audio out, AES out (or RS-422 data out, replaces AES), 4 SDI outputs

FRS-HD-SDI-R   SD/HD frame sync with high sensitivity 9/125um single mode optical input, internal audio handling and GPI I/O control, 4 SDI outputs

FRS-HD-DMUX-R   SD/HD frame sync with high sensitivity 9/125um single mode optical input, analogue stereo audio out, AES out (or RS-422 data out, replaces AES), 4 SDI outputs

2 Specifications

Optical SDI input

Data rate optical:	270 – 1485 Mbps
Sensitivity	
- HD-SDI (1485 Mbps):	Better than -20dBm
- SD-SDI (270 Mbps):	Better than -22dBm
Detector overload threshold:	Min. -3dBm
Detector damage threshold:	>+1dBm
Optical wavelength:	1200-1620nm
Transmission circuit fiber:	9/125um Single Mode
Connector return loss:	>40dB w/ SM fiber
Connector:	SC/UPC

Electrical SDI input

Connectors	75 Ohm BNC
Equalization	Automatic;
	- >300m @270Mbps w/Belden 8281, with BER < 10E-12
	- >100m @1485Mbps w/Belden 1694A, with BER < 10E-12
Input Return loss	>15dB, 5MHz -1.5GHz
Jitter tolerance	SD limit:
	- 10Hz-1kHz: >1 UI
	- 10kHz – 5MHz: >0.2 UI
	HD limit:
	- 10Hz-100kHz: >1 UI
	- 100kHz–10MHz: >0.2 UI

Electrical Sync input

Connector	2x 75 Ohm BNC
Format	Black & Burst, Tri-level
Input Return loss	>35dB @ < 10MHz,
	30dB @ < 30MHz
Termination	Selectable internal or external 75 Ohm termination(FRS-SDI-DMUX-C1 rev.2 or later only)
	75R termination on one of the sync inputs necessary on FRS-SDI-DMUX-C1 rev.1

Electrical SDI outputs

Number of outputs	4
Connectors	75 Ohm BNC
Output Return loss	>15dB, 5MHz -1.5GHz
Output signal level	800mV +/- 10%
Output signal rise / fall time 20% - 80%	- SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var.
	- HD limit: < 270ps, <100ps rise/fall var.
Amplitude overshoot	<10%
Output timing jitter	- SD: <0.2 UI
	- HD: <1 UI
Output alignment jitter	- SD: <0.15 UI
	- HD: <0.15 UI

Analog Audio output

Number of outputs	1 stereo pair
Connectors	2 x WECO audio connectors
Impedance	< 66R
Dynamic range	>100dB(A)
Crosstalk	< -60dB 20Hz-20kHz
THD+N	-70dB
Frequency response	20Hz-20kHz +/- 0.5dB
Maximum output level	24dBu +/- 1dB
Common mode DC immunity	0 – 48V
Level adjustment range	0 – 24dBu with 1db step
Two tone intermodulation	< -80dB

AES output

Number of outputs	1
Connectors	TP45
Return loss	110R +/-20% 0.1MHz – 6.144MHz
Output jitter	<0.0025UI peak

Supported standards

SD, 270 Mbps	SMPTE 259M, SMPTE 272M-AC
HD, 1485 Mbps	SMPTE 292M, SMPTE 274M, SMPTE 291M, SMPTE 296M, SMPTE 299M
Video switch point definition and sync	SMPTE RP168 (tri-level), SMPTE 170m, ITU-R. BT.470
AES	AES3-1996
Optical	SMPTE 297M, SMPTE 292M
EDH	Compliant to SMPTE-RP165
Video Payload Identification	SMPTE 352M-2002

Other

Power consumption	< 5W

- 4.5W/5V, 0.9W/15V, 0.0W/-15V with optics
- 3.5W/5V without optics

3 Description

3.1 Data path

HD/SD-SDI input is selected from either optical or electrical input and equalized, re-clocked and de-serialized and transferred to a processing unit called an FPGA. In the FPGA the signal is first sent through a *de-glitcher* that cleans up errors that might appear on lines, for instance due to switching. After the video is de-glitched, it is sent along two paths; it is given to a *frame-store buffer*, and it is given to the *audio de-embedder*.

The 16 audio channels coming from the de-embedder are bundled **in pairs** and sent to an audio store buffer. The audio is fetched from the *audio store buffer* according to a user specified delay and sent to an *Audio Cross Point.* The audio out of the Audio Cross Point can be any pair of audio channels de-embedded from the incoming video stream, an internal 1 kHz sine or an internal "black sound". "Black sound" is in function mute, but it produces a waveform pattern on the AES output which is different from mute. From the cross point outputs each channel pair enters an A*udio Processing Block*, where the paired channels may be shuffled. After the audio processing block the audio enters the *Audio Embedder*.

The video (with audio still inserted) is fetched from the frame buffer with the user specified delay and sent to a *Video processing block* followed by an *EDH processing block*. After the EDH block the video and audio is embedded according to the user settings and the video is sent from the FPGA to a serializer that re-clocks the data and output the SDI to a buffered output switch.

The buffered output switch is a 2x2 cross point with input 1 being the equalized and re-clocked input (non-processed) and input 2 being the output of the video processing. The two outputs are sent to two paired (non-inverting and inverting) outputs.

There are also outputs for one stereo pair of analog audio and one AES. These outputs are taken out from the Audio cross point and can be any stereo pair of audio channels embedded on the incoming video stream, the internal 1 kHz sine generator or the internal "black sound" generator.

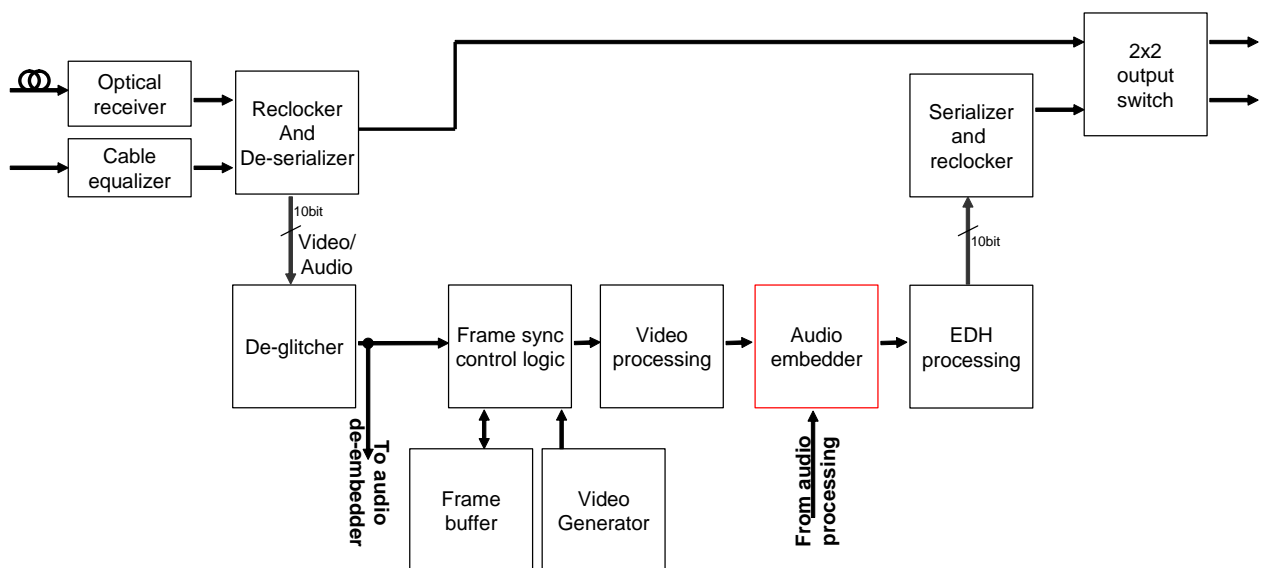## 3.2 Video blocks overview

Figure 2: Video function blocks

3.3 Optical/ Electrical input selection

The FRS-HD-DMUX has both an optical (option, see Chapter 1.1) and an electrical input. The input can be chosen either by an automatic selection with priorities and rule of switching or by manual selection. This feature is only available through GYDA.

Automatic selection mode

In GYDA the *video in mode* choice is set to auto. Three input choices can be made for three priorities; optical, electrical or mute. This priority sets the order in which the card will look for a valid input.

It is also possible to set a *rule* for when the input should be switched to the next priority. The rules are:

- lol = loss of lock
- los = loss of signal
- EDH = Errors are found in the video

Hold time and lock time can also be set for signals. This is described in Chapter 3.5.1.

3.4 De-glitcher

The de-glitcher corrects timing errors within a line. The de-glitcher has a 2048 samples buffer. When the first signal is present, we call it the "initial phase signal", data is taken from the centre of this buffer. If the timing reference of the video signal changes, when for instance a new source being switched into the signal path, the timing errors occurring by this change will be corrected if the new timing reference is within +/-1024 samples of the "initial phase signal". This also goes for all consecutive timing references.

If a signal occurs that is more than +/-1024 samples off relative to the "initial phase signal", the output will repeat the last frame, refill the 2048 samples buffer and take out data from the centre of the buffer. This new signal is now considered the "initial phase signal".

Hence, it produces an error free video output without frame wrapping when the video input comes from a router with synchronous input video signals that all lies within +/-1024 samples of each other.

3.5 Frame synchronizer

The frame synchronizer consists of a frame store buffer and some control logic. The frame store buffer can store up to 8 full HD frames. Data is fetched from this buffer according to the user settings by force of the control logic. The control logic sets the frame synchronizer into different modes dependent on the presence of a sync input.

3.5.1 Frame sync mode
If a sync input (B&B or Tri-level) is present, the frame synchronizer will output a signal that has a delay relative to this signal. Two parameters can be set; "**Phase delay**" and "**Video delay**".

Phase delay	0	lines	0	samples		
Video delay	2	frames	0	lines	0	samples

Figure 3: Gyda view of the video delay settings

Let us first focus on the *phase delay*, which also may be called "output phase delay". This parameter can be positive or negative, and determines the relationship between the

outgoing video and the sync signal. The parameter really determines a delay on an internal sync signal, isync[1]. The output is synchronous with isync, see Figure 4.
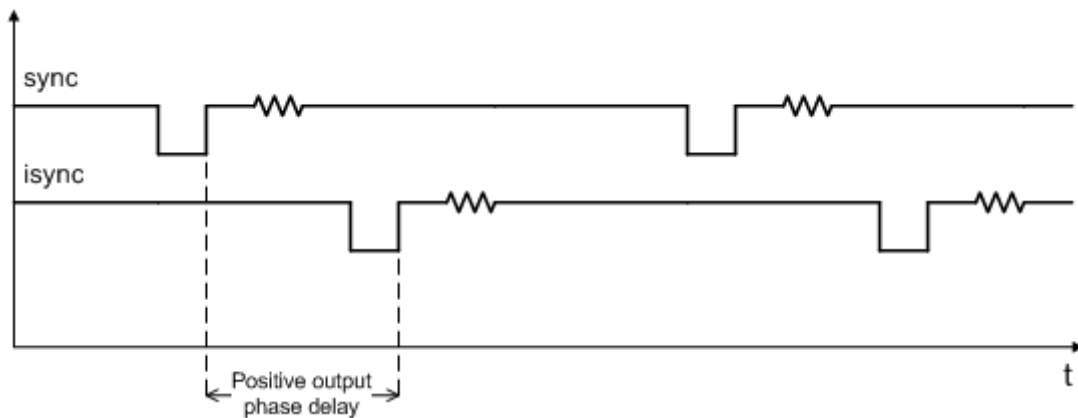

Figure 4: Positive phase delay

Figure 4 show how the sync signal and the isync signal would look on an oscilloscope, if converted to analogue signals. The delay of isync can be given in frames, lines, and samples. The delay can be negative, see Figure 5.
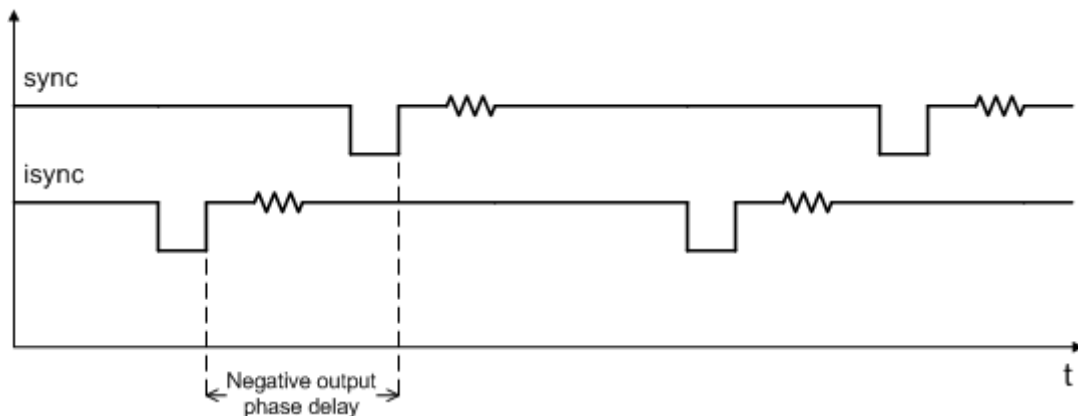

Figure 5: Negative phase delay

The *phase delay* can thus be written in several ways, a large positive delay will equal a small negative delay, because there is wrap-around on a frame basis. It follows that it is not useful to specify a *phase delay* larger than 1 frame. Strictly speaking the range could have been limited to -1/2 frame to 1/2 frame. For convenience, the delay range is allowed to be from -1 frame + 1100 samples to 1 frame – 1100 samples.

In order for FRS-HD-DMUX to honor the *phase delay* setting, it should ideally delay the incoming video between 0 to 1 frames. Because the processing delay through the card is 2 lines minimum, the actual window is between 2 lines and 1 frame + 2 lines. Hence, with the parameter (minimum) *video delay* set to 2 lines (the least number possible for the parameter); the output video will be between 2 lines and 1 frame + 2 lines delayed, with respect to the incoming video. A common occurrence in practical use is to synchronize an incoming video with a sync, but to let the outgoing video lead some samples or lines to the sync. This can easily be accomplished. Say that we want the outgoing video to occur 50 samples before the sync. We will then set the *phase delay* to -50 samples, and the *video delay* parameter to 2 lines. For convenience, let us assume

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[1] Note that *isync* is not a physical entity, but a term used in this context to explain the delay process and the use of the configurable parameters related to this process.

that the incoming video is iso-synchronous, but that it lags 20 lines after the sync. We will then have the situation shown in Figure 6.

Note that the numbers in circles in the next figures are visualizing the video frames.
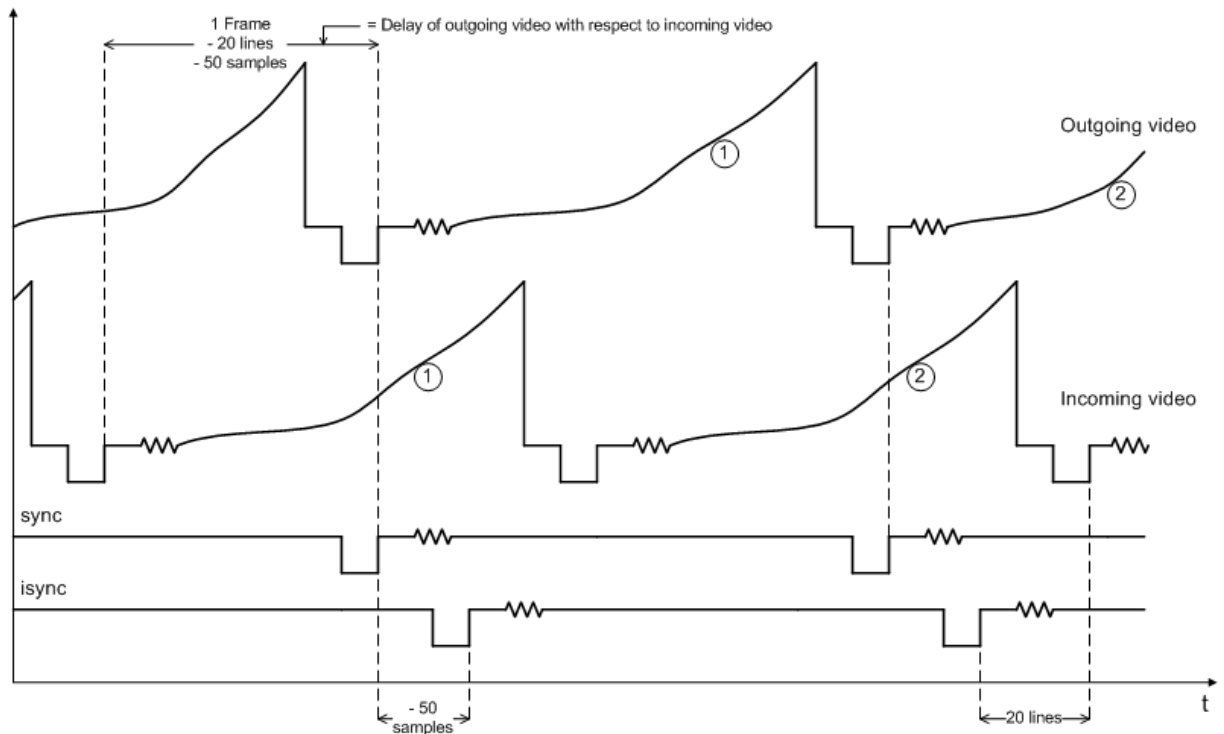
Figure 6: Example of delayed outgoing video

To match larger processing delays, one will want to first delay the incoming video, and then synchronize the video. This is equivalent to introducing a delay line for the incoming video, and then synchronize the output of the delay line with sync. In effect, one moves the delay-window start; this is equivalent with setting of the *video delay* to a larger value.

Let us assume that the *video delay* is set to 2 frames, 200 lines. In that case the outgoing video will be between 2 frames + 200 lines and 3 frames + 200 lines delayed with respect to the incoming video. For convenience, let us assume that the incoming video is iso-synchronous, but that it lags 25 lines after the sync. Let us also assume that the *phase delay* is set to -60 samples. We will then have the situation shown in Figure 7.
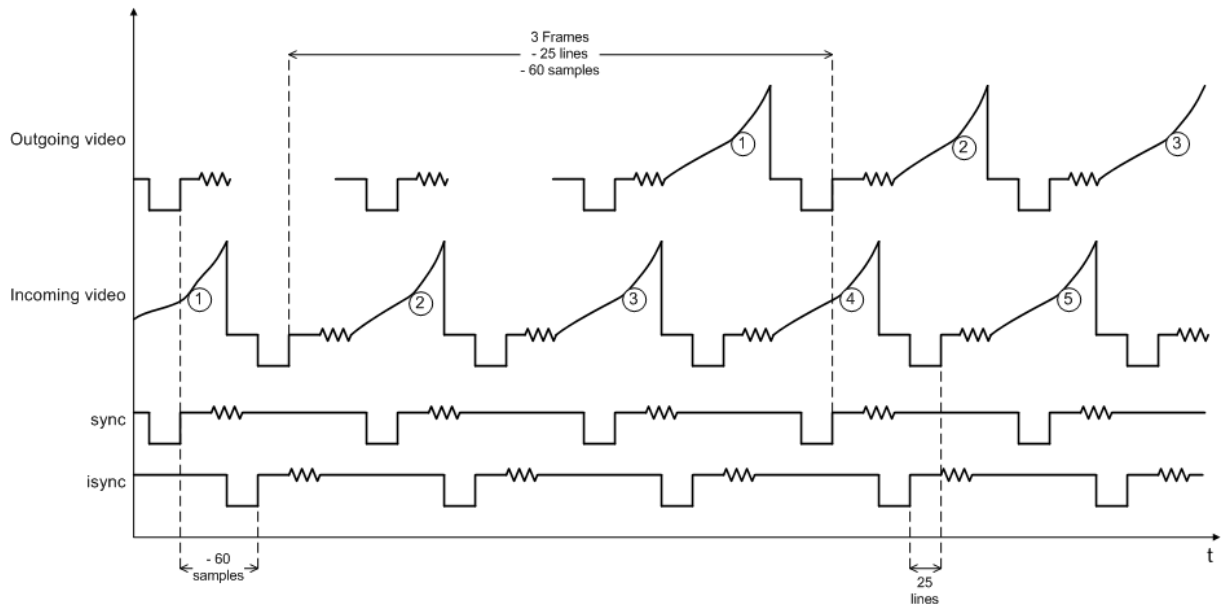
Figure 7: Another example of delayed outgoing video

To reiterate: The *phase delay* can be both positive and negative and sets the difference between the phase of the sync input and the video output. The *video delay* sets the delay between video output and video input. However, the actual delay might be longer as it also needs to phase up to the sync input. The actual delay may be up to 1 frame longer than the minimum video delay.

> The user may specify a *video delay* between 2 lines (min) and 7 frames (max).

The two parameters allow a user to delay the incoming video, and reference it to the sync input. By this mechanism, the user can precompensate processing delay in other equipment. The *video delay* setting simply determines a lower limit to a 1 frame wide window into a long delay line. The *phase delay* may be seen as a specification of the delay between the sync input, and a signal "isync". The output video is always synchronized to isync. A few more examples:

Example 1: The SDI input signal is isosynchronous to a sync signal, but 12 lines, 0 samples delayed. The *video delay* is set to 1 frame, 0 lines and 0 samples. The *phase delay* is set to 65 samples. The actual delay between the input video and the output video will be 2 frames - 12 lines + 65 samples.

Example 2: The SDI input signal is asynchronous to the sync signal (the frame frequency is slightly different). The *video delay* is set to 1 frame, 13 lines and 0 samples. The *phase delay* is set to -1 line. The actual delay will gradually change between 1 frame and 13 lines to 2 frames and 13 lines. The output will appear 1 line (in the output video format) ahead of the sync signal.

Example 3: The SDI input signal is isosynchronous to the sync signal, but 12 lines ahead of the sync signal. The *video delay* is set to 1 frame, 0 lines and 0 samples. The *phase delay* is set to -2 lines. The actual delay between the input video and the output video will be 1 frame + 10 lines.

The frames and lines are measured in units of the output SDI video standard. If the output SDI standard is 1080i25, a delay of one line is equal to 35.5us. If the output SDI standard is 720p50, a delay of one line is equal to 26.6us. If the output SDI standard is 625i25, a delay of one line is equal to 64us.

For a scenario where the card receives different HD video standards, (e.g. 1080i25 and 720p50) the user may want to conserve a specific delay in microseconds for all HD video standards. This is accomplished by specifying the delay in number of samples instead of frames and lines. (For HD video standards the sample frequency is equal over standards, but the line and frame frequencies are different for the different standards).

If video input disappears

Given that stable SDI input and sync input exists: If the SDI input disappears, the picture will freeze for 1 second and then go to black video if the card is in the default configuration.

It is possible to change the freeze time (hold time in GYDA). The black video can also be changed to color bar, check field or flat field video through Gyda.

When the SDI input disappears, the Frame Delay pulses at the back plane will also disappear.

If video input reappears

Given stable sync input, the video will reappear after 1 second of locked video input if card is in default settings. It is possible to change the time before reappearance. This variable is labeled lock time in GYDA.

If sync input disappears

Given that stable SDI input and sync input exists: If the sync signal disappears, the card will act as in frame delay mode, see Chapter 3.5.2.

NOTE: This will result in a frame roll as the delay changes.

If sync input reappears

Given that a stable SDI input exists: If the sync signal reappears the delay mode will change back to Frame Sync mode. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

If both signals disappears

The picture will first freeze for 1 second, and then go to color bar. The output is now referenced to the local clock source. The local clock source has been synchronized with the previous seen incoming sync, and remains stable as long as operating conditions (such as temperature) does not change materially. Under stable conditions, the clock source is accurate to within 1ppm of the last sync source, but the generator is not a reference generator.

3.5.2 Frame delay mode
In this mode a sync signal is not present. The delay set is then directly related to the incoming video. 1 frame and 1 line delay, means that the output will be 1 frame and 1 line delayed version of the input.

If video signal disappears

The picture will first freeze for 3 seconds and then go to color bar. The output is now referenced to the local clock source. However this clock source will be kept within 1 ppm of the last video source.

If video signal reappears

If the input video signal reappears the video will reappear on the output after 3 seconds of stable input video. The delay will be set to the same delay as before loosing input.

NOTE: This may cause a frame roll.

If a sync input appears

Given that a stable SDI input exists: If a sync signal appears the delay mode will change to Frame Sync mode, see Chapter 3.5.1. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

3.6 Video generator
The video generator can produce different simple signals: Color bar, Check field and flat field.

The flat field is possible to set up with all luma and chroma values.

The generator may be used as the video source if there is no video signal present at either of the video inputs. The generator may also be switched on with GYDA. This will override video input but the generator signal will be locked to the input.

The video standard of the generator may be set with GYDA but only if there is no video input present.

3.7 Video processing block

The video processing block consists of a *gain and offset* adjustment, and a video payload *legalizer*.

3.7.1 Gain and offset

The gain and offset adjustment is done separately on the Y, Cb and Cr samples.

	Range Gyda
Luma gain	0 – 32767 (0-4x, 1x = 8192)
Chroma gain	0 – 32767 (0-4x, 1x = 8192)
Luma offset (gain =1)	-4095 – 4095
	(-511.75 – 511.75 in sample values)
Chroma offset (gain = 1)	-2047 – 2047
	(-255.75 – 255.75 in sample values)

3.7.2 Video payload legalizer

The legalizer hard clips the upper and lower limit of the video payload. With the legalizer enabled these limits are:

Upper limit	Luma:	3ACh
	Chroma:	3C0h
Lower limit	Luma:	040h
	Chroma:	040h

With the legalizer disabled, the video processing block hard clips both luma and chroma to 3FBh and 004h.

3.8 EDH processing block

If enabled, the EDH processing block extracts the EDH package from the video, updates the EDH flags according to SMPTE RP165 and inserts the EDH package into the ancillary data of the video.

If disabled, The EDH processing block only reads, process and report the EDH package without changing it in video stream.

3.9 Video output selection

The board has four outputs where two and two can be either routed directly from the re-clocker or routed through the processing unit. In GYDA the direct path is labeled *thru* and the processing path is labeled *processed*.
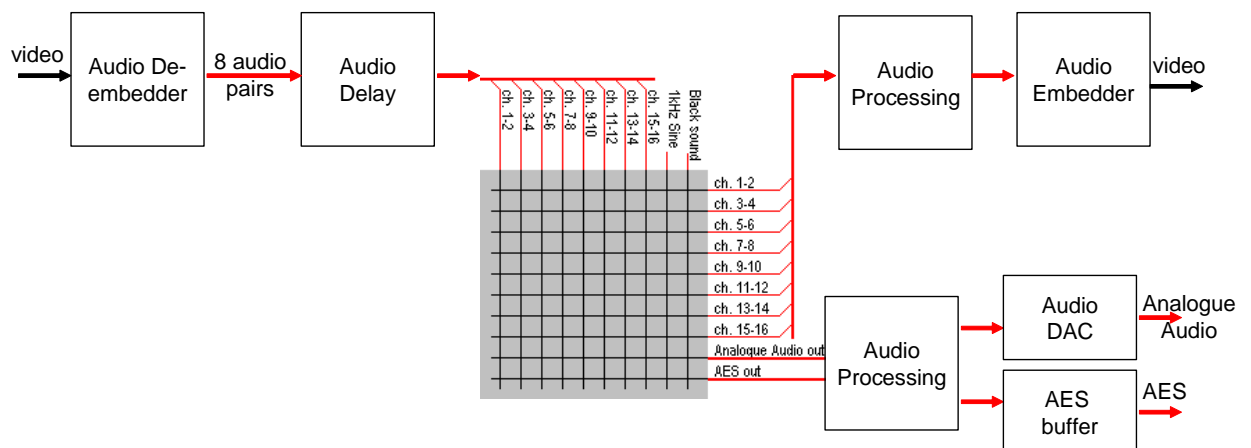
3.10 Audio blocks overview

Figure 8: Audio function blocks

3.11 Audio de-embedder

The Audio de-embedder extracts all audio embedded in the video stream. The de-embedder is always enabled.

3.12 Audio delay

An audio delay relative to the video output can be specified commonly for all de-embedded channels. This is done in GYDA. The audio delay is specified in audio samples relative to the output video, and can be both positive and negative.

NOTE: As the audio delay is relative to the video output it is possible to specify an audio delay that will be an actual negative delay. This will cause audio errors.

The negative audio delay is limited by the positive video delay. Since the audio delay is always relative to the video, the only way to give the audio a negative delay is to delay the video by a positive amount. To go beyond this limit would require the audio to be re-embedded before it had even been de-embedded from the incoming video, and that is of course impossible.

The positive audio delay is limited by the fact that the sum of the video delay and the relative audio delay cannot be larger than 32000 audio samples (approx. 0.67 ms with 48 kHz audio). If the video delay is set to minimum, the full 32000 audio samples will be available, but if the video delay is set to – say – 5 frames, the maximum relative audio delay is reduced to 20000 audio samples (assuming 25 frames per second, 5 frames equals 0.2 seconds, which in turn equals 12000 audio samples, and 32000-12000=20000). When doing these calculations, remember that if a sync reference is present, a video delay setting of N frames means that the actual video delay can vary continuously between N and (N+1) frames. The calculations should therefore be based on (N+1) frames.

3.13 Audio cross point matrix

The audio cross point matrix is a 10x10 cross point with inputs and outputs as shown in Figure 8. The 8 de-embedded channels, a 1 kHz sine and "black sound" are selectable inputs. "Black sound" is explained in Chapter 3.1. The outputs of the cross points are 8 stereo channels for re-embedding, one analog audio output and one AES output.

All outputs have fallback options that can be set in GYDA. The priorities can be selected between *matrix* (being the choice in the cross point matrix), *sine* or *black.*

3.14 Audio generator

The stereo audio generator is available in the audio cross point matrix as a source. It is a high purity 1 kHz sine wave with a 250ms interruption on the left channel every 3 seconds. The audio level may be set to one of two standards. The two levels are -18 dBFS and -20 dBFS. These two levels correspond to EBU R68 and SMPTE RP 155.

3.15 Audio processing block

The output of each stereo signal from the audio cross point matrix may be manipulated in the audio processing block (LL, RR, RL, !LR, L!R, (L+R)/2, MS) This is controlled with the GYDA controller.

The stereo signals may be output in one of the following ways:

- LR, Left / Right	No change.
- LL, Left/ Left	Left channel is copied into the right channel.
- RR, Right/ Right	Right channel is copied into the left channel.
- RL, Right/ Left	Channels are swapped.
- !LR, ØLeft/ Right	The left channel is phase inverted.
- L!R, Left/ ØRight	The right channel is phase inverted.
- (L + R)/2	The left and right channels are summed.
- MS	The left and right channels are converted from AB stereo to MS stereo.

The sum products ((L+R)/2 and MS) are reduced in level by 6 dB to avoid any possibility of clipping.

3.16 Audio embedder

The audio embedder can be enabled per group in GYDA. When a group is disabled the audio inside that group is removed.

When in SD mode, a 24bit sound signal can be changed to 20bit through GYDA control. This removes the 4 least significant bits of the signal. The audio control package is left unchanged as the bit range is still present.

The audio control package can also be switched on and off in SD mode through GYDA control.

The audio embedder can be switched off all together. In this state the audio embedded on the input signal is left unchanged.

3.17 Analog audio output

The level of the analog audio output can be adjusted in GYDA. The minimum step is 0.5dB and the range is from -95.5dBu to 24dBu. It is also possible to mute the output totally.

4 Configuration

The board can be configured both manually and through the Nevion control system *GYDA*. However, only a few of the configurable parameters are available when operating in manual mode.

4.1 Manual mode

To reach manual mode DIP16 labeled OVR on the board must be switched on (to the right) and the board must be re-booted. This takes the board out of GYDA control (if it was previously set to off) and onto being controlled by the DIP switch and rotary switch settings. Settings not controlled by any of these switches are set to settings from previous settings (factory setup or GYDA setup).

The Manual Mode configuration controls are all found on the front side of the board. There are two sets of DIP switches, one rotary switch and two push buttons. On the bottom side of the card, three slide switches can also be found, but they are hardware switches that are set for all operation modes.
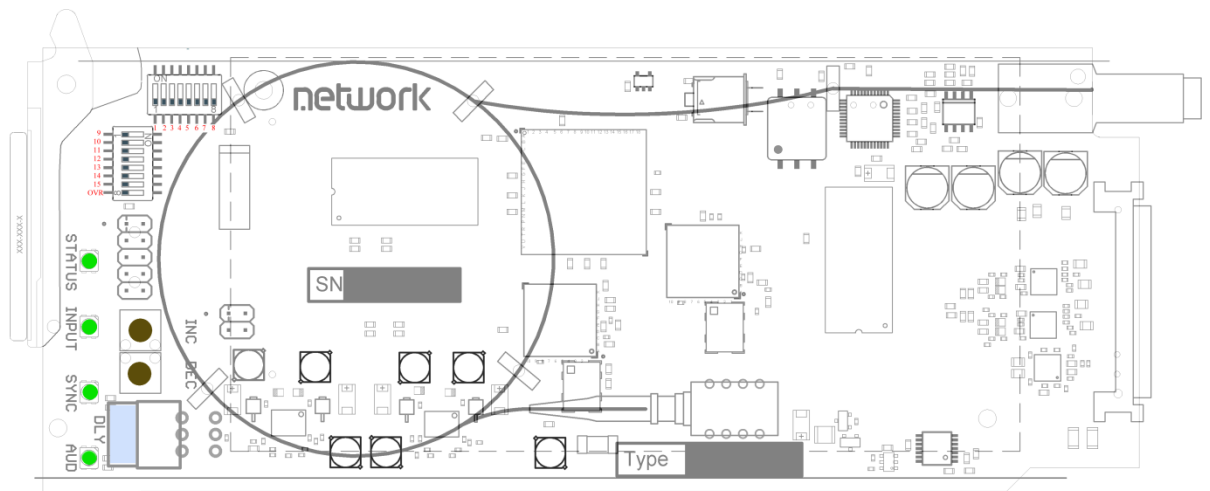
Figure 9: The figure shows a top view component printout of the board. Note the location of LEDs, push-buttons, the rotary switch and the 2 sets of DIP-switches.

4.1.1 DIP switch functions

The two sets of DIP switches are labeled with a number running from 1 to 15. The 16th DIP is labeled *OVR.*

Note that the left DIP switch of the horizontal DIP package is number 1. The top DIP switch of the vertical DIP package is number 9.

Table 1:   DIP SWITCH FUNCTIONS

Switch #	Function name	Function DIPs	Comment
1 - 2	ADAC group	DIP[1 2] = [Off Off] => Emb grp 0 DIP[1 2] = [Off On] => Emb grp 1 DIP[1 2] = [On Off] => Emb grp 2 DIP[1 2] = [On On] => Emb grp 3	These 3 DIPS routes one embedded AES channel to the Analog Audio output
3	ADAC ch1/ch2	Off = ch1, On = ch2 (of group selected from DIP1&2)	
4 - 5	AES group	DIP[4 5] = [Off Off] => Emb grp 0 DIP[4 5] = [Off On] => Emb grp 1 DIP[4 5] = [On Off] => Emb grp 2 DIP[4 5] = [On On] => Emb grp 3	These 3 DIPS routes one embedded AES

Switch #	Function name	Function DIPs	Comment
6	AES channel	Off = ch1, On = ch2 (of group selected from DIP4&5)	channel to the AES output
7	Emb. enable	Off: No audio embedded On: Audio embedded	When off, the audio is left untouched on the SDI stream. When on, the audio configured to be embedded is embedded into the SDI.
8	Dlink/ AES	Off: Data link on AES output. On: AES on AES output.	With Data link selected, note that the two slide switches on the bottom side must be switched.
9 - 11	Frame delay	DIP[9 10 11] = [Off Off Off] => 0 frms DIP[9 10 11] = [Off Off On] => 1 frms DIP[9 10 11] = [Off On Off] => 2 frms DIP[9 10 11] = [Off On On] => 3 frms DIP[9 10 11] = [On Off Off] => 4 frms DIP[9 10 11] = [On Off On] => 5 frms DIP[9 10 11] = [On On Off] => 6 frms DIP[9 10 11] = [On On On] => 7 frms	With a sync-input present, this sets the minimum frames delay. Without a sync-input present this sets the no. of frames delay relative to the input.
12	SDI OUT 1	Off: through mode On: processed mode	In through mode the video only goes through a re-clocker.
13	SDI OUT 2	Off: through mode On: processed mode	In through mode the video only goes through a re-clocker.
14	Video Generator	Off: Color bar On: Black field	This is the video generator signal that is shown when video is detected lost according to the fallback rule set in GYDA.
15	RESET	Off: Use values preset by GYDA. On: RESET to factory defaults	This DIP is only read at power up. After repowering with the DIP off, the board must be kept in the frame for minimum 10s to fully reset. Values preset by GYDA, are only values not set by DIPs, push buttons or rotary switches.

Switch #	Function name	Function DIPs	Comment
16	OVR	Off: GYDA mode On: Manual mode	This DIP is only read at power up. OVR is short term for GYDA override

FACTORY reset function

The factory reset is done by setting DIP 15 to *On* and power up the card. The inputs (optical, electrical video and sync) should be removed. Then, pull out the card, put DIP 15 to *Off* and power up the card again. The card will now reset. The board must be under power for at least 10 seconds for all the values to reset.

4.1.2 Rotary switch and push buttons

The *rotary switch*, labeled DLY, adjusts the *phase delay* by -5 to +4 video lines. It is only functional when a sync signal, black & burst or tri-level, is present at the sync input. The rotary switch is accessible from the board front.

The *push buttons,* labeled INC and DEC, are used to fine adjust the *phase delay* by samples. It can adjust +/- ½ video lines for the present video standard.
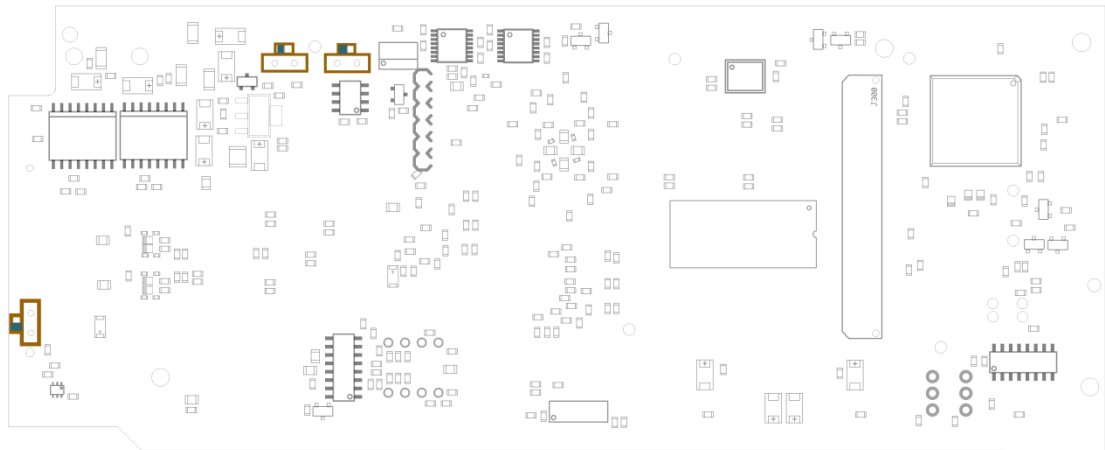
Figure 10: The figure shows a bottom view component printout of the board. Note the location of the slide-switches.

4.1.3 Slide switches

The two switches at the top of Figure 10 switch between AES out and Data out. It DC couples the output signal when in DATA out mode, and AC couples the signal when in AES mode.

> Note that it is also necessary to enable the data output on DIP8 (=Off), or in GYDA to output embedded data. Switches moved to the right routes out AES.

The switch on the left card edge switches between backplane sync input and Flashlink distributed sync (Future feature upgrade of Flashlink frame). Switch moved up routes the backplane sync to the card.

4.2 GYDA mode

All functions of the card can be controlled through the GYDA control system. The GYDA has an information page and a configuration page.

4.2.1 Information page

The information page shows a dynamic block-diagram of the board and some additional information text. The block diagram updates with the boards status, showing input signal selected, signals missing (by red crosses over signal lines) and routing through switches. It also shows the audio matrix selections that have been made in the configuration page.

> Note that if embedded audio is missing in groups the user will still be allowed to select the input in the matrix, but the output will go to a fallback position. This will be shown in the block-diagram only with a red cross over the input line to the matrix.

The text on the information page gives information about functionality not displayed on the dynamic block diagram.

The *video delay* represents the actual delay between input and output video.

The audio de-embedder 1-4 shows the state of the audio control package for the embedded audio on the input signal.

The audio embedder 1-4 shows the state of the audio control package and the bit depth for the embedded audio on the output signal.

Embedded part shows the data rate of data embedded in the audio control package on the incoming signal.
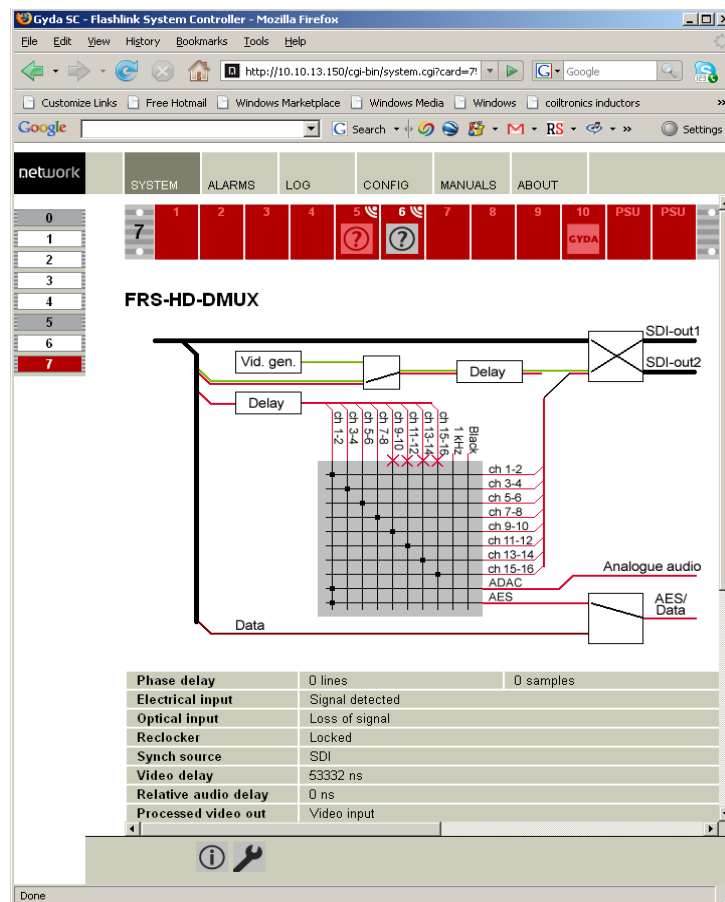

Figure 11: GYDA information page

4.2.2 Configuration page

The different configuration possibilities are explained in detail in Chapter 3, under the corresponding functions.
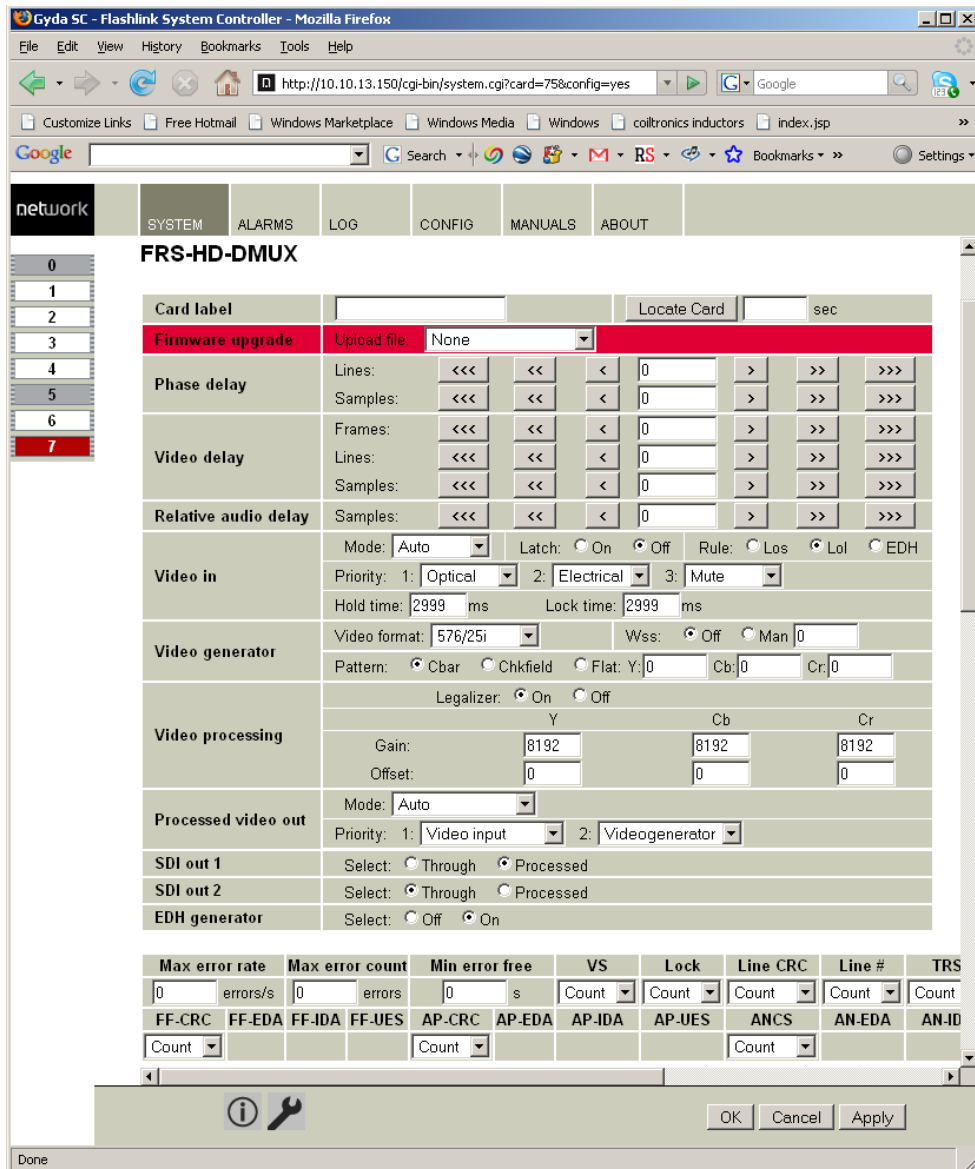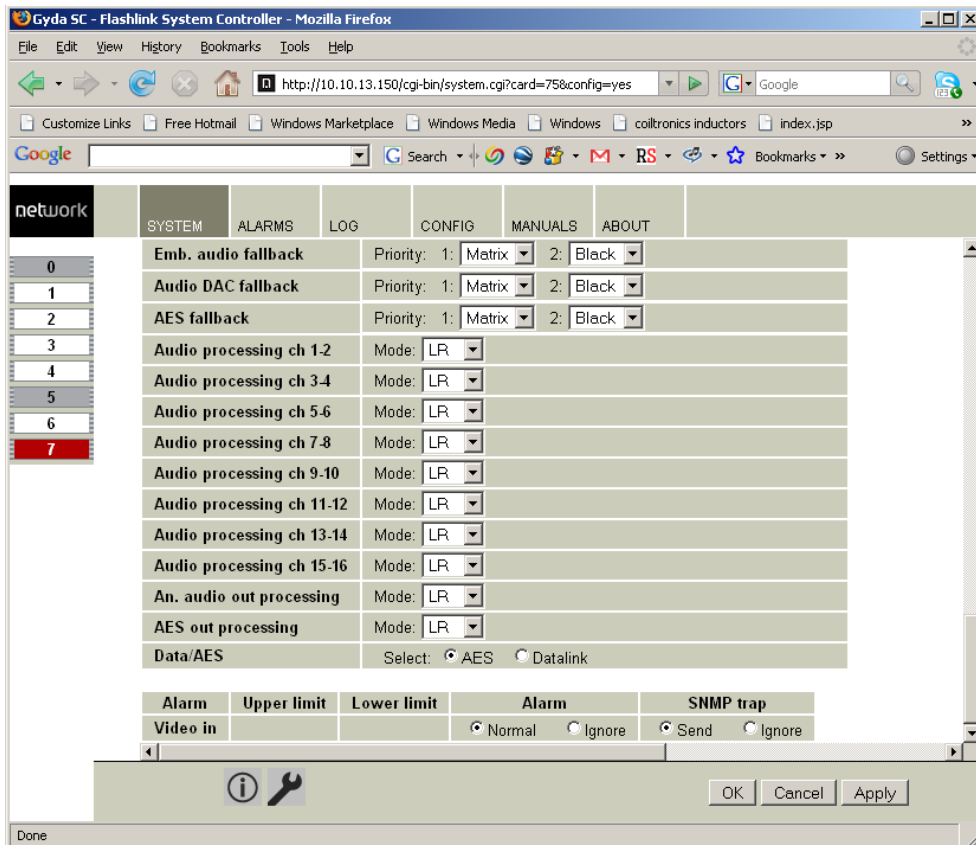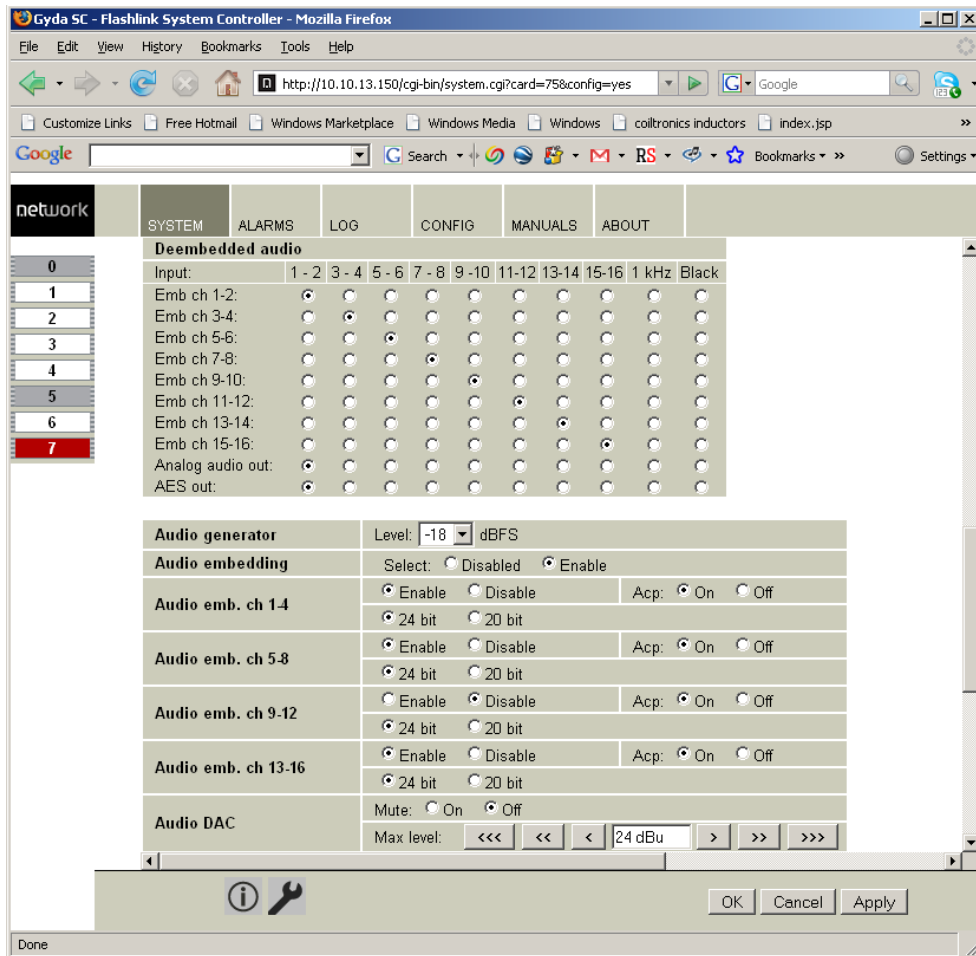
Figure 12: Configuration page (3 screen dumps at different positions on the page)

5 Connections
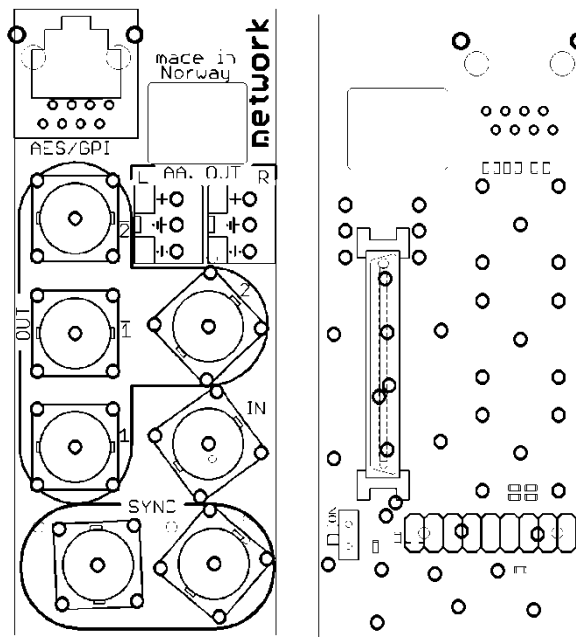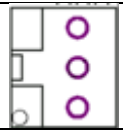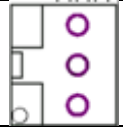
Figure 13: FRS-HD-DMUX-C1 (this is rev.2 of the backplane)

The backplane for the FRS-HD-DMUX is labeled FRS-HD-DMUX-C1. The table below shows the connectors and their functions.

> It is important to terminate the sync input. The backplane opens for looping the sync. It is then necessary to terminate the last board in the loop.
> On boards of revision 2 or later this can be done either by setting the slide switch position to ON (on backplane) or by adding a 75R terminator to one of the sync input.
> On boards of revision 1 termination is done by adding a 75R terminator to one of the sync inputs.

Function	Label	Connector type		
HD/SD-SDI input	IN	BNC		
HD/SD-SDI output 1	1	BNC		
HD/SD-SDI output 1 inverted	$\overline{1}$	BNC		
HD/SD-SDI output 2	2	BNC		
HD/SD-SDI output 2 inverted	$\overline{2}$	BNC		
Sync input	SYNC	BNC		
Sync input (Termination or loop-thru)	SYNC	BNC		
Analog audio out left channel	AA.OUT L	WECO Audio connector		
			O	Positive
			O	GND
			O	Negative
Analog audio out left channel	AA.OUT R	WECO Audio connector		
			O	Positive
			O	GND
			O	Negative
GPI out 1-3	No label	TP45 pin 1, 2 ,3 (8 = GND)		
AES out	No label	TP45 pin 4, 5, 6		
Frame delay pulse	No label	TP45 pin 7 (8=GND)		
Optical input	No label	BSC-II (for SC input)		

6 Operation

6.1 Front panel LED indicators

Diode \ state	Red LED	Orange LED	Green LED	No light
Card status	PTC fuse has been triggered or FPGA programming has failed	Module has not been programmed or RESET and OVR DIPS are on.	Module is OK	Module has no power
SDI input status	Video signal absent.	Video signal present but card not able to lock VCXO	Video input signal in lock	Module has not been programmed
Sync input status	Sync signal absent	Sync signal present but card unable to lock VCXO	B&B or Tri-level sync in lock	Module has not been programmed
Audio input status	No audio embedded in incoming video	One, two or three audio groups embedded in incoming video	4 audio groups embedded in incoming video	Module has not been programmed

6.2 GPI alarms

Only three alarms are present on the RJ45 connector as two pins are used for the AES/ RS422 data port and one pin is used for Frame delay pulse signal.

The three alarms are:

- Status error
- Video signal lost
- Black and burst lost

An active alarm condition means that the transistor is conducting.

6.3 GPI/ AES/ Data connections 8pin modular jack

Pin number	Description
1	Status error
2	SDI input lost
3	Black & Burst lost
4	AES+/RS422+
5	Ground
6	AES-/RS422-
7	Frame delay
8	Ground
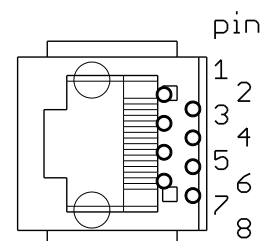
Figure 14: GPI pin layout

6.4 RS422 commands

6.4.1 FLP4.0 required commands

Block	Blk #	Commands	Example	Response	Control
-	-	?	?	*product name* SW rev *n.m* FW rev *r.s* protocol ver 4.0\	**Hello command.** *Note 1: No other commands will be available until the card has received this hello.* *Note 2: This command will also enable checksums.* *Note 3: Cards are designed to be hot-swappable. To sync with the start of a new command, the cards will wait for a <lf> character before looking for a valid command.*
conf	0	-	conf 0	*too long to list*	**Configuration settings** Retrieves the card's configurable settings. Each addressable block is represented by a single line. Dynamic status *may* be included in response, but is usually reported in *info* only.
-	-	info	info	*too long to list*	**Dynamic status info** Blocks with static settings only will usually not be included, see *conf* above.
-	-	chk off	chk off	ok	**Checksum off** If issued twice in succession, this command will disable checksums. Note: Responses will still have the checksums appended. *NOTE1: ? command turns the checksum on again*
-	-	locate on <seconds> locate off	locate on 3 locate off	ok	**Card locator** This command will cause all the LEDs to flash for a user specified number of seconds. If omitted, the value <seconds> will be set to a default of 120 seconds. The flashing can be terminated at any time with *locate off*.
-	-	address	address	address <address>	**Card address** This command will check and update the card's current rack and slot address, which is normally only done at start-up.
-	-	filename	filename frshddmux-0-105.ffw filename frshddmux-0-100.mfw	<name>'.'<extension>	**Firmware update** The <name> part must match the card's hardware and include a revision number, and the extension must be either 'ffw' for FPGA firmware or 'mfw' for microcontroller firmware. After running this command the board will wait for the firmware in Intel-hex format.
-	-	fin	fin	ok	**Finalize** Finalize the programming of the microcontroller. See description of the uC bootloader (separate document).
misc	0	-	NOT AVAILABLE BY COMMAND. ONLY FOUND in Conf 0	prog | fin ' ' | ovr	**Misc info** *prog* if the card is freshly programmed by the bootloader and the program is still un-finalized. *fin* is the normal condition. *ovr* if DIP-switch 16 is set to the ON position and the card is under DIP-switch

| | | | | | control.
Note 1: The info part of misc has additional functionality when locate is used: *locating <remaining seconds>*. This enables a visible countdown clock in Gyda, but is not a required part of FLP400. |

6.4.2 Normal control blocks

Block	Blk #	Commands	Example	Response	Control
pin	0	on | off	pin 0 on pin 0 off	cd | ncd	Pin diode for optical input. No control; only used to report *carry detect* or *not carry detect*.
ceq	0	-	ceq 0	cd | ncd	Cable equalizer for electrical input. No control; only used to report *carry detect* or *not carry detect*.
cho	0	pri <k> | pri <k> <l> | pri <k> <l> <m> pos man <k> | pos auto latch on | latch off| latch reset rule lol | rule los | rule trse t1 <hold_time> t2 <lock_time>	cho 0 pri 0 cho pri 0 1 cho pri 10 2 cho 0 pos man 1 cho 0 pos auto cho 0 latch on cho 0 latch off cho 0 latch reset cho 0 rule lol cho 0 rule los cho 0 rule trse cho 0 t1 1000 cho 0 t2 1000	size 3 pri *k,l,m* auto latch <latch_status> t1 <hold time> t2 <lock time> <rule> size 3 pri *k,l,m* man *m* latch <latch_status> t1 <hold time> t2 <lock time> <rule>	**Video input select** ***pri:*** a prioritized list of inputs, used when change-over is automatic. The list can have 1, 2 or 3 entries, or *levels*. Manual mode is effectively the same as automatic mode with one priority level only, but has its own command. 0 = from optical input 1 = from electrical input 2 = generator (from cho 1) ***latch:*** <latch_status> can be either *on* or *off* and selects if the change-over is latching or not, used when change-over is automatic. Latch on means that if we've lost our main source and moved on to a lower priority level, we'll not search to see if the higher pri's will reappear. **rule:** <rule> can be either *los, lol* or *trse*, which means *l*oss *o*ff *s*ignal, *l*oss *o*f *l*ock, and *t*iming *r*eference *s*ignal *e*rror. This determines what triggers an automatic change-over. ***t1*** **and** ***t2:*** change-over doesn't happen immediately, as a precaution against glitches and unstable signals. The timers t1 and t2 let the user decide how long (in ms) we will cling on to a missing input before we consider it gone and move on to the next pri level, and how long an input with a higher priority should be present before we consider it repaired and switch back, respectively. *Note 1: the latch setting only applies to rule los.* *Note 2: the card change back to physical inputs from generators* <u>*regardless*</u> *of latch setting. As a side note, this means that t2 is important even when rule=lol and/or latch is on.* *Note 3: If we have selected rule=lol and a 3-level pri list with two physical inputs on top and a generator at the bottom and*

					we're in generator mode (lost both physical inputs) and both physical inputs reappear at more or less the same time, which physical input will be chosen is unpredictable. This again due to having one reclocker only and having to hunt for a valid input in the background while the generator is still selected.
cho	1	pri <k> | pri <k> <l> pos man <k> | pos auto	cho 1 pri 0 cho 1 pri 0 1 cho 1 pos man 1	size 3 pri *k,l* auto size 3 pri *k,l* man *m*	**Video fallback setting** Second video change-over. This cho is a slave of cho 0, in the sense that it has no latch, t1, t2 or rule settings of its own. It has a generator input that must be set up separately and that allows a switch to an internal video generator. 0 = from cho 0 1 = from video generator, vgen 0 2 = kill *Note: manual mode is the same as automatic mode with a priority list with only one priority level.*
cho	2-11	pri <k> | pri <k> <l>	cho 2 pri 1 cho 5 pri 0 2	size 4 pri *k,l*	**Audio fallback setting** Audio change-over blocks, one cho per audio output from the audio matrix, mtx 0. No other settings but the priority list. 0 = from audio matrix 1 = sine 2 = black 3 = kill *Note: Only generators (pri 1, 2 or 3) are allowed to be set as first and only priority.*
cho	12	pri <k> | pri <k> <l>	cho 12 pri 1 cho 12 pri 0 2	size 4 pri *k,l*	**Audio common fallback setting** A short-cut to set change-overs 2-11 all at once. Will of course not report anything in info, that's left to the individual cho blocks.
cho	13	pos man <k>	cho 13 pos man 0 cho 13 pos man 1	size 2 man *k*	**AES output select** This cho has only manual mode and works as a simple 2:1 switch. 0: AES is selected 1: Embedded UART is selected
cho	14	pos man <k>	cho 14 pos man 0 cho 14 pos man 1	size 2 man *k*	**EDH insert select** This cho has only manual mode and works as a simple 2:1 switch. 0: EDH off 1: EDH on
cho	15	pos man <k>	cho 15 pos man 0 cho 15 pos man 1	size 2 man *k*	**SDO 0 output select** This cho has only manual mode and works as a simple 2:1 switch. 0: Through mode (re-clocked only) 1: Processed mode (SDI from FPGA
cho	16	pos man <k>	cho 16 pos man 0 cho 16 pos man 1	size 2 man *k*	**SDO 1 output select** This cho has only manual mode and works as a simple 2:1 switch. 0: Through mode (re-clocked only) 1: Processed mode (SDI from FPGA
cho	17	pos man <k>	cho 17 pos man 0 cho 17 pos man 1	size 2 man *k*	**Audio embedding enable** This cho has only manual mode and works as a simple 2:1 switch. 0: embedding off (Audio embedded on

					input signal left untouched) 1: Embedding on
rcl	0	-	rcl 0	lock | lol	Reclocker. No control; only used to report *lock status*.
emb	0-3	en | dis acp (on | off) use24 (on | off) del (off | (on <del12> <del34>))	emb 0 en emb 2 dis emb 1 acp on emb 3 acp off emb 1 use24 on emb 2 use24 off emb 0 del off emb 2 del on 54 -432	(en | dis) use24 (on | off) acp (on | off) del (off | (on <del12> <del34>))	**Audio embedder block** **en/dis:** Enables or disables the embedding of the group into the ancillary area. **acp on/off:** This is valid only for SD and enables the audio control package. **use24 on/off:** This is only valid for SD and selects between 24bit and 20bit sound. **del off/on delay12 delay34:** For each of the embedder groups the delay bits for ch1+2 and for ch3+4 can be inserted into the ACP. The delay value can be positive and negative and is put directly into the ACP as it is written. *Note: To set both delays to 0 would be the same as turning the delays off. The response reflects this.*
demb	0-3	-	demb 0 demb 2	grp *k* en	**Audio de-embedders** One permanently assigned to each incoming group, always enabled. No control available.
vprc	0	lglz on | lglz off (y | cb | cr) <gain> <offset>	vprc 0 lglz on vprc 0 lglz off vprc 0 y 8192 0 vprc 0 cb 2000 0 vprc 0 cr 1000 1000		**Video processing block** Gain and offset are both signed fixed point numbers. Gain is in 2.13-format, while offset for Y and the chroma channels are given in 10.2 and 9.2 respectively. Gain range is $0 - 32767$, $\text{Gain}_{=0x} = 0$, $\text{Gain}_{=1x} = 8192$, $\text{Gain}_{=4x} = 32767$ Luma Offset range is $-4095 - 4095$, $\text{Offset}_{=0} = 0$ Chroma Offset range is $-2047 - 2047$, $\text{Offset}_{=0} = 0$
sync	0	-	sync 0	'lol' | ('lock' ('trilvl' | 'bb' | 'sdi'))	Frequency reference for video output. Status only, no commands available.
dly	0	<frames>frms <lines>lines <samples>sps	dly 0 2frms dly 0 2lines 30sps dly 0 0frms 50sps dly 0 0frms 3lines 50sps	'tgt' <frames> frms <lines> lines <samples> sps	**Video delay** This sets the minimum video delay of the card. In info this block reports back the current delay in nanoseconds. This will vary with the incoming video standard.
dly	1	<audio_samples>sps	dly 1 -30sps	'tgt' <audio_samples> sps	**audio delay** The audio delay is given in audio samples. Audio delay is always given relative to video.
dly	2	<lines>lines <samples>sps	dly 2 1lines -30sps	'phase' <lines> lines <samples> sps	**Video phase** If lines != 0 the resulting phase will vary with incoming video standard, see dly 0 above.
vgen	0	cbar | chkfield | white | yellow | cyan |	vgen 0 cbar	video <lns>/<rate><scan> wss (auto| off | (on <wss_value>)) (cbar | chkfield | white |	**Internal video generator.** The video generator will be activated in two different ways: If selected as a fallback option the generator will generate the selected pattern when the

		green | magenta | red | blue | black flat \<Y> \<Cb> \<Cr> video \<lns>/\<rate>\<scan> wss (auto|off | (on \<wss_val>))	vgen 0 flat 200 0 100 vgen 0 video 1080/24p vgen 0 video 1080/25p vgen 0 video 1080/25i vgen 0 video 1080/29i vgen 0 video 1080/30i vgen 0 video 720/24p vgen 0 video 720/25p vgen 0 video 720/29p vgen 0 video 720/30p vgen 0 wss auto vgen 0 wss on 7	yellow | cyan | green | magenta | red | blue | black | (flat \<Y> \<Cb> \<Cr>))	other input(s) are missing, and then use the video settings from the last external source present. It can also be selected as the main input in cho 1, in which case its own video settings will also be used.
edh	0	msk \<24b_mask> reset	edh 0 msk 0xFE0005 edh 0 reset	msk \<24b_mask>	**Error detection and handling** Error counting. The count itself is reported in info. Errors can be masked off and not counted; this is the purpose of the mask. The counter itself is 16b and will wrap around, but can also be reset by issuing *reset*.
mtx	0	\<i1> \<o1> ...\<iN> \<oN> \<i1> \<o1>,\<o2>,...\<oN> \<i1> \<o1> - \<o2> ..or the above combined	mtx 0 0 2 1 4 5 5 mtx 0 0 0, 1 1, 2 2 mtx 0 0 0-9 mtx 0 0 0 1 1 2 2-9	size M:N i1 i2 i3... iN	**Audio matrix** mtx 0 (size 10:10) controls the audio matrix; outputs 0-7 are embedded sound, 8=adac and 9=AES. *Note: Any combination of the three basic commands are allowed, for instance the following command to set up a 10x10 audio matrix in a single line:* *mtx 3 1 1 2 2 3 0,3-9* *=> mtx 3 size 10:10 3 1 2 3 3 3 3 3 3 3*
agen	0	lvl \<sine_level>cBFS	agen lvl -180 agen lvl -200	sine 1kHz lvl \<sine_level>cBFS	**Audio generator** The amplitude of the generated sine that can be chosen as fallback in audio change-overs. Legal values are -180cBFS or -200cBFS (centiBel referred to full scale output). Units are optional, but if included must be written as cBFS (case sensitive).
aprc	0-9	lr | rl | ll | rr | nlr | lnr | mm | ms	aprc 0 lr aprc 3 ll aprc 9 mm	lr | rl | ll | rr | nlr | lnr | mm | ms	**Audio processing** One block for each output from cho 2-11. Outputs 8+9 are adac and AES, the lower 8 are routed to the embedder. The meaning of the commands are as follows: lr = Normal rl = Channel swapped ll = Left channel to both output channels rr = Right channel to both output channels nlr = Left channel phase inverted lnr = Right channel phase inverted mm = Mono, both channels = (r+l)/2 ms = Mono/stereo, m=(l+r)/2, s=(l-r)/2
ablk	0	mute (on | off) lvl \<level>	ablk 0 mute on ablk 0 mute off ablk 0 lvl -500 ablk 0 lvl 30	dac lvl \<level>cBu mute \<mute_status>	**Audio DAC control** This word *dac* identifies this audio block as a DAC. The outputs can be muted, \<mute_status> given as *on* or *off*, and the output level can be set in cBu (tenth dBu). Units are optional, if included must be written as *cBu* (case sensitive). Note 1: The lvl and mute are independent, so that the card will remember the lvl setting (and change lvl setting) while muted.

Block	Blk #	Commands	example	Response	Control
					Note 2: The resolution of the lvl control is 0.5dB but the card will perform correct rounding to nearest legal value and report the resulting setting. Legal input range is [-957cBu, 247cBu], representing the range [-95.5dBu, 24.5dBu].
uart	0	-		tx	The embedded data link, selectable by cho 13. No control possible, the word tx indicates that this is a transceiver only. Uart info reports link status: *los* (loss of signal), *raw*, or the speed of the embedded link (example: *115200/8/n/1*).

6.4.3 Commands intended for debug/lab use only

Block	Blk #	Commands	example	Response	Control
spi	-	on | off	spi on spi off		spi off used to isolate the uC from the SPI lines during programming of the flash by external programmer. spi on must be issued in order to re-enable normal card operation with the uC as the SPI master.
spir	-	<address>	spir 0x0004		Read a single word (or byte) from a SPI registers. Addressing is 16b and most significant nibble determines which chip. These are the address ranges: 0x0000 – 0x0fff : audio DAC 0x1000 – 0x1fff : FPGA 0x2000 – 0x2fff : flash 0x3000 – 0x3fff : deserializer 0x4000 – 0x4fff : serializer 0x5000 – 0x5fff : shift register (for LEDs) 0x6000 – 0x7fff : Not in use on this module.
spiw	-	<address> <data>	spiw 0x0004 0x2c		With the same address ranges as for spir above, this command allows the user to modify SPI registers.
thebug	-	-	thebug		A collection of debug information that is presented in a Gyda block-like format. First line tells which image is currently loaded. Second line contains the filename and version of the uC software, including the AVR controller it was compiled for. The third line contains the SW flags in uC, the number of times the watchdog timr has kicked in, readout of dip-switches, input select for deserializer, SDOn on/off, slew rates, and status for the video changeovers. The next two lines contain raster information from the deserializer and serializer respectively, while the last two lines contain sample values for mlines and VCXO.

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
   - Operating room temperature range: 0°C to 45°C
   - Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:
   - Temperature range: -10°C to 55°C
   - Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the "Administrative Measure on the Control of Pollution by Electronic Information Products". In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

組成名稱 Part Name	Toxic or hazardous substances and elements					
	鉛 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
FRS-HD	O	O	O	O	O	O
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.						
X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.						

This is indicated by the product marking:

A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site http://www.nevion.com/. Please contact Nevion's Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.