# ARC-SD-XMUX4

SD-SDI Aspect Ratio Converter
with 4x AES I/O

# User manual

Rev. B

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## Revision history

Current revision of this document is the uppermost in the table below.

| Rev. | Repl. | Date | Sign | Change description |
|---|---|---|---|---|
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| | | | | |
| B | 1 | 2015-05-14 | MB | Cover page update; DoC removed; no other changes to content |
| 1 | 0 | 2011-11-02 | TB | Added chapter 6.2 on GPI alarms and GPI inputs |
| 0 | A | 2011-03-04 | SHH | Initial revision. |

# Contents

# 1 Product overview

The Flashlink ARC-SD-XMUX4 converts the aspect ratio of an SD-SDI signal. The module changes the scaling during the vertical blanking period so that the changes appear to be instantaneous.

The ARC-SD-XMUX-4 has 4 x SDI outputs and 4 x AES I/Os.

The ARC-SD-XMUX4 is also a frame synchronizer with an adjustable offset relative to the sync signal.

The ARC-SD-XMUX4 also has a de-glitcher to give error-free synchronous switching.

The audio embedded in the SD-SDI stream is de-embedded and can be delayed relative to video. The stereo audio channels can be swapped in the audio matrix before they are re-embedded in the SD-SDI data output stream.

A selection of user parameters of the card can be controlled by switches on the board. Complete control of all parameters is available by use of the Flashlink RS422 Control Protocol Version 4, which is supported by the Multicon GYDA system controller from software release 2.13.

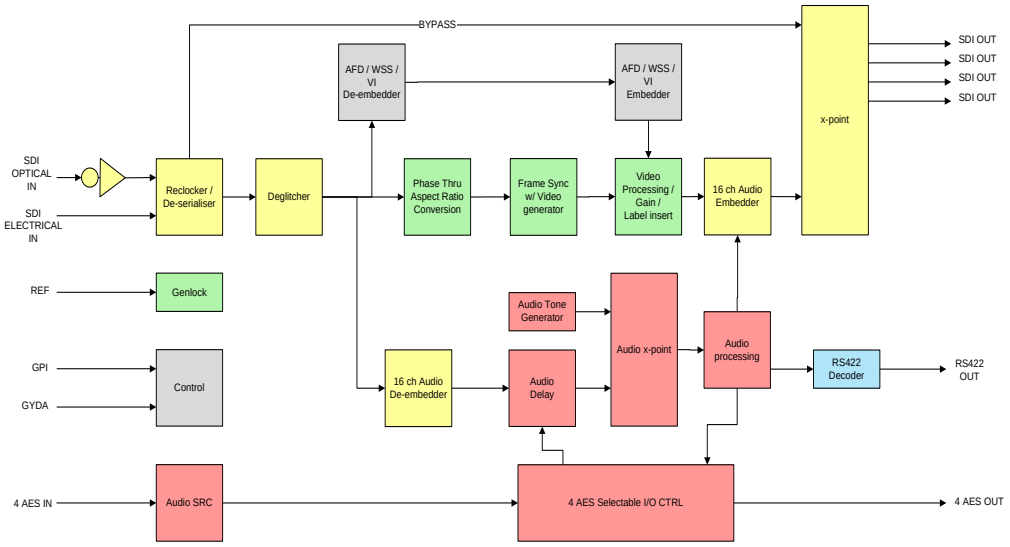



**Figure 1: ARC-SD-XMUX4-R block diagram.**

## 1.1 Product versions

| | |
|---|---|
| ARC-SD-XMUX4 | SD-SDI aspect ratio converter. 4AES I/O, 4 SDI outputs and frame synchronizer functionality. |
| ARC-SD-XMUX4-R | As above but with a high sensitivity 9/125µm single mode optical input. |
| ARC-SD-XMUX4-R-L | As above but with an APD 9/125um single mode optical input |

# 2 Specifications

**Optical SD-SDI input**

| | |
|---|---|
| Data rate: | 270 Mbps |
| Sensitivity: | Better than -20dBm (PIN)/-30dBm (APD) |
| Detector overload threshold: | -3dBm |
| Detector damage threshold: | >+1dBm |
| Optical wavelength: | 1200-1620nm |
| Transmission circuit fiber: | 9/125um Single Mode |
| Return loss: | >40dB w/ SM fiber |
| Connector: | SC/UPC |

**Electrical SD-SDI input**

| | |
|---|---|
| Connectors | 75 Ohm BNC |
| Equalization | Automatic:<br>- >300m @270Mbps w/Belden 8281, BER < 10E-12 |
| Input Return loss | >15dB, 5MHz -1.5GHz |
| Jitter tolerance | - SD limit:<br>- 10Hz-1kHz: >1 UI<br>- 10kHz – 5MHz: >0.2 UI |

**Electrical Sync input**

| | |
|---|---|
| Connector | 75 Ohm BNC |
| Format | Black & Burst, Tri-level |
| Input Return loss | <-35dB @ < 10MHz,<br>30dB @ < 30MHz |
| Termination | Selectable internal or external 75 Ohm termination |

**Electrical SD-SDI outputs**

| | |
|---|---|
| Number of outputs | 4 |
| Polarity | 2 non-inverting, 2 inverting |
| Connectors | 75 Ohm BNC |
| Output Return loss | >15dB, 5MHz -1.5GHz |
| Output signal level | 800mV +/- 10% |
| Output signal rise / fall time, 20% - 80% | - SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var. |
| Amplitude overshoot | <10% |
| Output timing jitter | - SD: <0.2 UI |
| Output alignment jitter | - SD: <0.15 UI |

**AES output**

| | |
|---|---|
| Number of inputs/outputs | 4 |
| Connectors | WECO |
| Return loss | 110R +/-20% 0.1MHz – 6.144MHz |
| Output jitter | <0.0025UI peak |
| Impedance | 110 ohm transformer balanced |
| Input audio data rate | 24 kHz to 100kHz, converted to 48 kHz uf not isochronous to either SDI input or sync input. |
| Embedded audio word length | 24 bits |
| Embedded audio Channels status | As received when isochronous, otherwise fixed. |

**Supported standards**

| | |
|---|---|
| SD, 270 Mbps | SMPTE 259M, SMPTE 272M-AC, SMPTE297M |
| Analog video | SMPTE 170M, SMPTE 274M, ITU-R. BT.470, |
| Centre of picture definition | SMPTE RP187, ITU-R. BT.470 |
| Aspect ratio preservation | SMPTE RP199-1999, SMPTE RP221 |

| | |
|---|---|
| Video switch point definition and sync | SMPTE RP168 (tri-level), SMPTE 170M, ITU-R. BT.470 |
| AES | AES3-1996 |
| Optical | SMPTE 297M |
| EDH | Compliant to SMPTE RP165 |
| Video Payload Identification | SMPTE 352M-2002, SMPTE 2016-1, SMPTE2016-3, SMPTE RP186 |

**Minimum video signal delay through processing**

| | |
|---|---|
| Minimum delay | 256 lines |

**Other**

| | |
|---|---|
| Power consumption | +5V DC/ 5W max |
| W/o optical input module | -0.3W |
| All AES configured as inputs (unused) | -0.5W |

# 3 Description

## 3.1 Data paths

The SD-SDI input selected from the optical or electrical input is equalized, re-clocked and de-serialized and transferred to a processing unit (FPGA). In the FPGA the signal is sent through a *de-glitcher* that cleans up erroneous video lines, for instance due to switching. After the de-glitcher the video is sent to the *Audio de-embedders*, where audio is split from the video.

### 3.1.1 Audio data path

The stereo audio channels from the de-embedder are sent to an audio store buffer. The audio is fetched from the audio store buffer after the user specified delay. It is then sent to the *Audio matrix.*

Two other sources are available in the audio matrix: A 1 kHz stereo sine tone and a generated *black sound* which is a legal audio stream with muted audio.

Depending of how many of the configurable AES I/Os have been designated as inputs, there may also be up to four AES inputs available in the matrix.

Outputs with missing inputs are routed to a fallback signal. The fallback signal may be silence or the tone generator.

Each output from the matrix is sent to an *Audio Processing Block* where channels can be processed or rearranged within the channel pair.

Finally, eight stereo pairs are routed to the *Audio Embedder*. Depending on how many of the four AES I/Os have been designated as outputs, up to four stereo pairs are also routed the AES outputs.

### 3.1.2 Video data path

The video is routed to an *aspect ratio converter block* and the resulting SD video is passed to a *Frame synchronizer block*.

An internal video generator can be switched in as a fallback source if the input video is missing.

The audio is re-embedded and the video then passes through a *Video processing block* with an integrated *Legalizer*, before entering an *EDH processing block.* Embedding of the EDH packet is configurable.

The parallel video is sent out from the FPGA and into a serializer that re-clocks the data and sends the SDI to a buffered output switch.

The output switch is used to bypass the video processing core so that DVB-ASI may pass through the module. The switch selects between the FPGA output (*Processed* mode) and video that has only been re-clocked (*Through* mode).

## 3.2 Video blocks overview

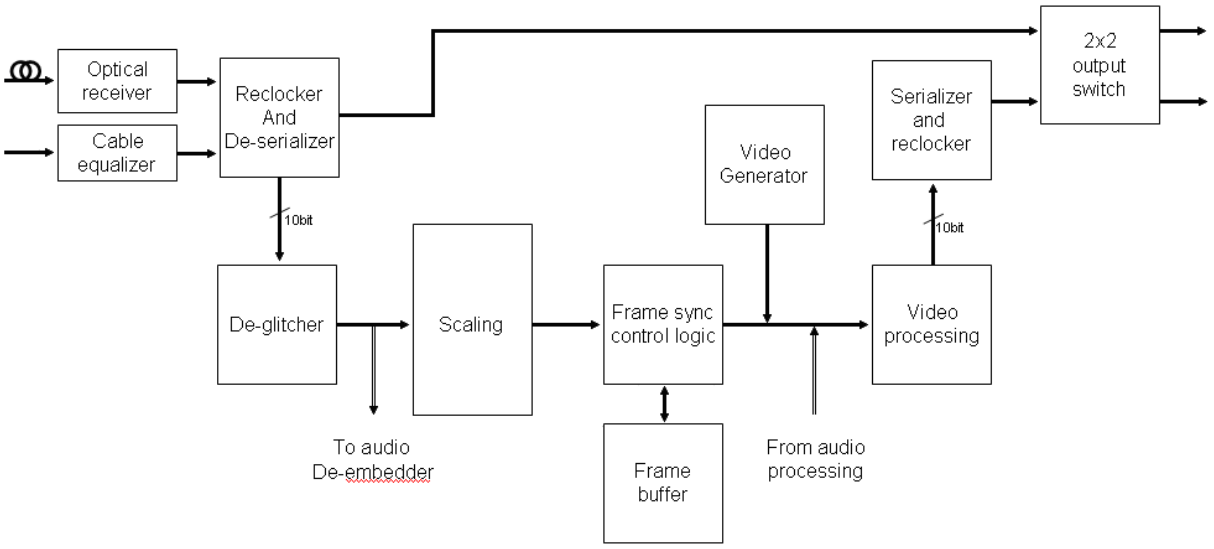



**Figure 2: Video block diagram**

## 3.3 Optical/ Electrical input selection

The ARC-SD-XMUX4-R has both an optical and an electrical input. The active input can be selected either:

1. Automatically based on a prioritized list of inputs and a rule of switching.
2. Manually.

When controlled by DIP switches, the card will use the fall back source and generator settings saved from the last Multicon GYDA session.

### 3.3.1 Automatic selection mode

*Video in Mode* set to *auto*: There are three priority levels. Each level may be assigned an input setting; optical, electrical, video generator or mute.

The priority is the order in which the board will look for a valid input. The card will switch to the next priority after a loss of lock to the input signal.

If the active input is either electrical or optical, and the other is selected as the first priority (main), the module will not switch back to main unless signal is lost on the active channel, or the user hits the *Latch reset* button.

*Hold time* determines how long a signal has to be missing/out of lock before it is considered lost. This is useful to avoid switching when the input has intermittent faults.

*Lock time* determines how long a higher prioritized signal has to be locked before it again can be considered to be present and stable. This is only active when the module has lost both optical and electrical video inputs.

**If video input disappears**

Given that stable SDI input and sync input exists: If the SDI input disappears and *Video in* is set to *Auto*, the board will hold on to the current input for the time set by *Hold time* whilst frame freezing.

The board will then select the next input in the priority list (or go up to the main input, if no fallback exists).

### 3.3.2 Manual selection mode

If the SDI signal disappears the board will frame freeze indefinitely.

## 3.4 De-glitcher

The de-glitcher corrects timing errors within a line of video due to source switching. This allows perfect synchronous switching.

Non-synchronous switching *can* result in a frame that is split between the old and the new video, but the output will always be continuous.

## 3.5 Aspect Ratio Converter block

The aspect ratio converter block is a 13 tap high quality linear resampling scaling engine. It may be used to stretch or shrink a picture vertically and horizontally. The picture may also be offset with respect to the centre of the picture.

The block can detect a change in aspect ratio information embedded in the input signal and change the scaling during the vertical blanking period allowing on-air automatic switching of aspect ratio conversion.

Externally triggered changes of aspect ratio are also deferred until the next vertical interval to allow the use of the module in a transmission signal path.

The module is intended to be used primarily to convert SD video between standard aspect 4:3 and widescreen 16:9.

The primary difficulty with the conversion is the sheer number of possible conversions. This can be greatly reduced by setting the output aspect ratio to be 4:3 or 16:9. We call this the **output environment**. The actual scaling will then depend on the input signal.

The **output environment** setting actually describes the aspect ratio of the pixels. The **fill factor** is the term for the amount that the picture fills the output frame, the presence of horizontal or vertical curtains or black bars.

The output signal will have the appropriate AFD, VI WSS and S352M embedded. All of these metadata types may also be disabled.

There are four operational modes for the module:

1. AFD -> Frame fill setting -> default conversion
2. AFD -> default conversion
3. Frame fill setting -> default conversion
4. Fixed default conversion

The primary assumption for the first three modes is that an input signal with the same aspect ratio as the output environment *will not be scaled.* (There are a couple of exceptions if the picture has both horizontal and vertical curtains.)

The scaling that is set in default conversion will be used for all input signals.

### 3.5.1 Automatic scaling modes

The following applies to the first three automatic modes of operation.

The scaling performed by the module is determined by the input picture aspect ratio and fill factor (presence of ‘curtains’) but normal SD video does not natively state what aspect the pixels are or if another conversion has already been applied. There are three sources of information that *may* be present in the video that can provide some or all of this information.

Active Format Descriptor (SMPTE 2016, referred to as AFD) and Video Index (SMPTE RP186 referred to as VI) describe both the aspect ratio and the fill factor of the picture.

However, the fill factor descriptor *may* contain a code to indicate that the fill factor of the picture is unknown. In that case, the code for the input aspect ratio is used.

SMPTE352M is a data packet that can be used to identify the aspect ratio of the picture.

Wide Screen Signaling present in the input video (WSS) can also be used to identify the aspect ratio of the incoming picture. The trouble is that WSS codes are by themselves indistinguishable from WSS Extended codes, but have a completely different meaning. This means that the user must select if WSS should be interpreted as WSS or WSS-Ext, and if this selection does not match the choice made in the equipment that inserted the WSS information, the resulting scalings will seem unpredictable.

**Mode 1: Full automatic mode**
The aspect ratio control block will start by looking for AFD presence in the input signal to select the aspect conversion. If that is not present it will look for VI, then WSS and finally SMPTE S352M information. If no aspect ratio information is present in the video, the default scaling setting will be used.

When a valid format descriptor is present, either from AFD or VI, all the conversions in the AFD code drawing are possible for the given output environment.

In the case where only input environment information is available, a subset of the conversions is used. The desired filling method must be set. This may be one of the following:

- Protect input frame : No cropping. Full curtains.
- Zoom to fill frame : The image will be cropped and zoomed to fit. No curtains.
- 14:9 : The image will be zoomed and cropped. Narrow curtains (pillar or letter box).

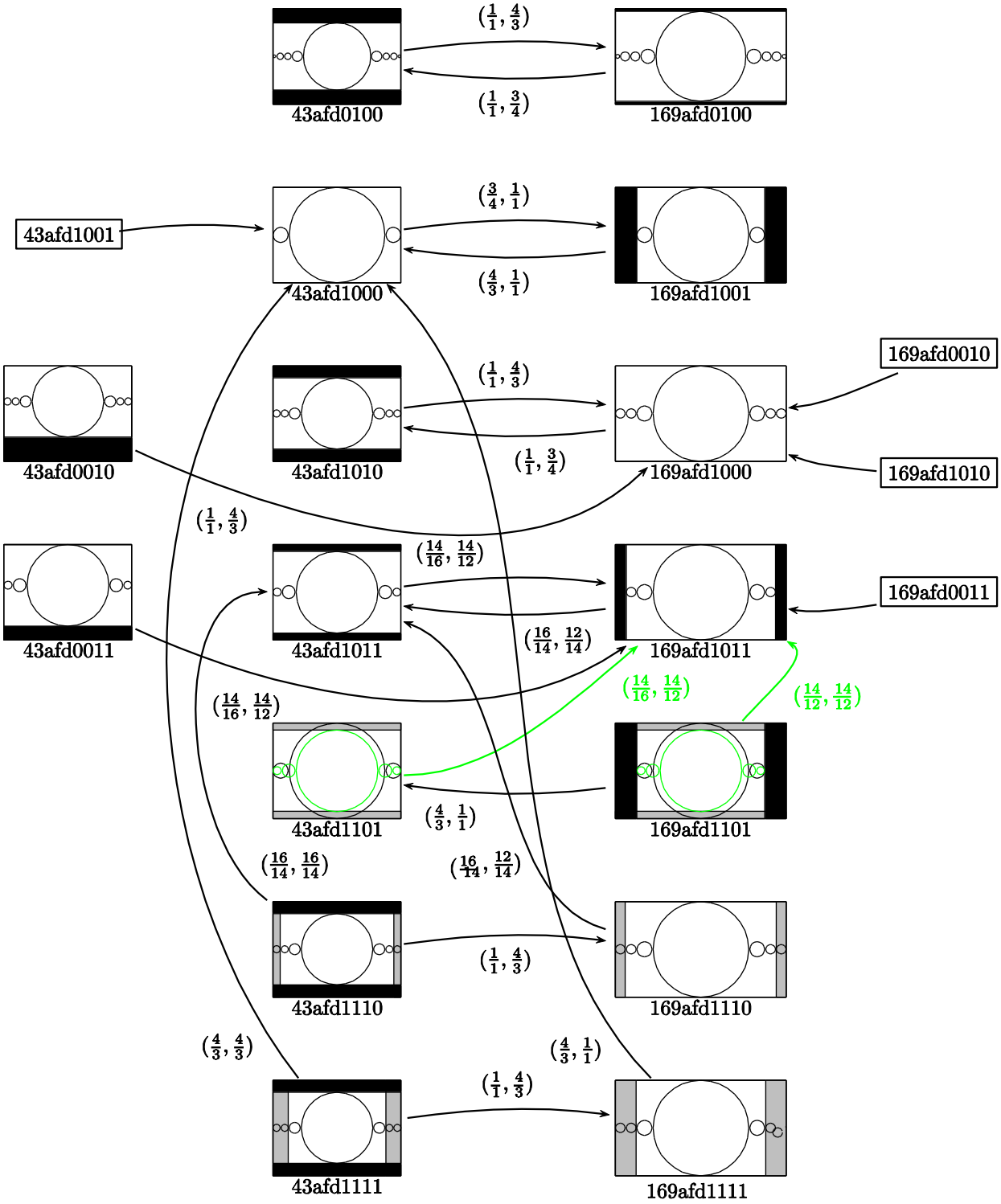
If the input environment is the same as the output environment, no conversion will be performed.

**Mode 2: AFD or default**
This mode will only use the AFD information if present. The default scaling will be used if there is no AFD packet, no video index and no WSS, or if the active format descriptor is set to ‘Unknown’.

**Mode 3: Fill mode or default**
This mode will only use the input aspect information from the AFD information if present. The S352M packet will be used if it is present and neither AFD packets, VI, nor WSS are present. The default setting will be used if there is no AFD packet, no video index, no WSS and no S352M packet.

**AFD conversions**

The figure below shows the different transitions that are defined. The incoming format is given by the VI/AFD, and the user has supplied wanted output environment. To avoid clutter, transitions from a state to itself are not shown in the figure. The corresponding AFD format is shown for reference.



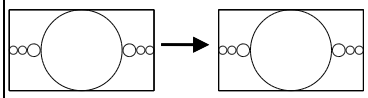
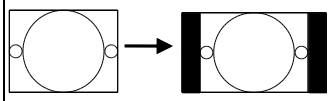
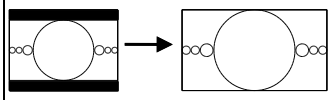
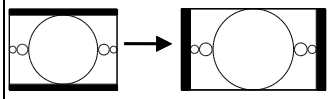
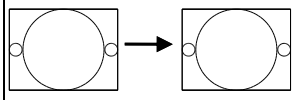
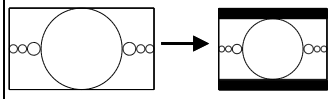
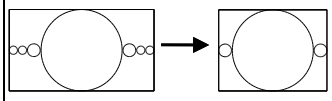
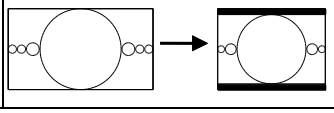

At first the figure looks confusing, but observe that each state have only one arrow leading from itself to the other column. The arrows define the normal conversion when the input environment is different to the output environment. Find the picture type that you have on the input and follow the arrow which points out of that state to find the conversion that will be performed by the ARC-SD-MUX when the AFD code is present.

There are a few states where the input picture has both horizontal and vertical curtains and these also have arrows within the same column. These are conversions that will be performed when the input environment is the same as the output environment.

**Fill mode conversions**
If the module cannot find any fill factor information but has aspect ratio information, it will perform one of three conversions when the input environment is different to the output environment.

1. Protect input frame.
2. Zoom to fill frame.
3. Zoom to 14:9.

The table shows the conversions that will be performed when this mode is active.

| Output Environment | Non-AFD Conversion | Input environment | Conversion performed |
|---|---|---|---|
| 16:9 | Any. | 16:9 |  |
| 16:9 | Protect input frame | 4:3 |  |
| 16:9 | Zoom to fill frame | 4:3 |  |
| 16:9 | 14:9 | 4:3 |  |
| 4:3 | Any. | 4:3 |  |
| 4:3 | Protect input frame | 16:9 |  |
| 4:3 | Zoom to fill frame | 16:9 |  |
| 4:3 | 14:9 | 16:9 |  |

### 3.5.2 Default scaling mode
This mode can be used to control scaling manually. The selected ‘default scaling’ will be used without regards for any incoming aspect ratio information.

The ‘default scaling’ field is also used as fallback in the automatic modes when no aspect ratio information is available (see automatic modes on the previous pages).

### 3.5.3 Selecting output environment and default scaling by GPI
There are 4 GPI input lines that can be controlled individually by external equipment, and therefore 16 different combinations. Each of these 16 states can be mapped to one of the scalings available under Default scaling. The GPI lines will then select the Default scaling,

which means that they will either control the active scaling directly (if the scaler is in Default scaling mode) or the fallback scaling that will be chosen when no AFD/VI/WSS/SMPTE352 information is available in the automatic modes.

The GPI lines can also be made to control the output environment. By selecting from the left part of the matrix, the output environment will be set to 4:3. Conversely, it will be set to 16:9 by selecting from the right part.

It is also possible to map one or more states to “No action”, which means that the card will simply ignore this GPI condition. This option can be particularly useful if a subset of the GPI values is used and the external equipment is unable to switch all four GPI lines simultaneously. Although the GPI lines are de-bounced (filtered), unintended states could theoretically be visited by the GPI lines in a transition from one intended value to another. It is therefore recommended to map all unused states to “No action” to get the cleanest possible switch between scalings.

Information about the currently selected default scaling and output environment is stored in the card (and also the system controller Multicon). If a restart occurs (from loss of power) the latest settings will be recalled from non-volatile memory even if the GPI lines should now be in a state that is mapped to ‘No action’.

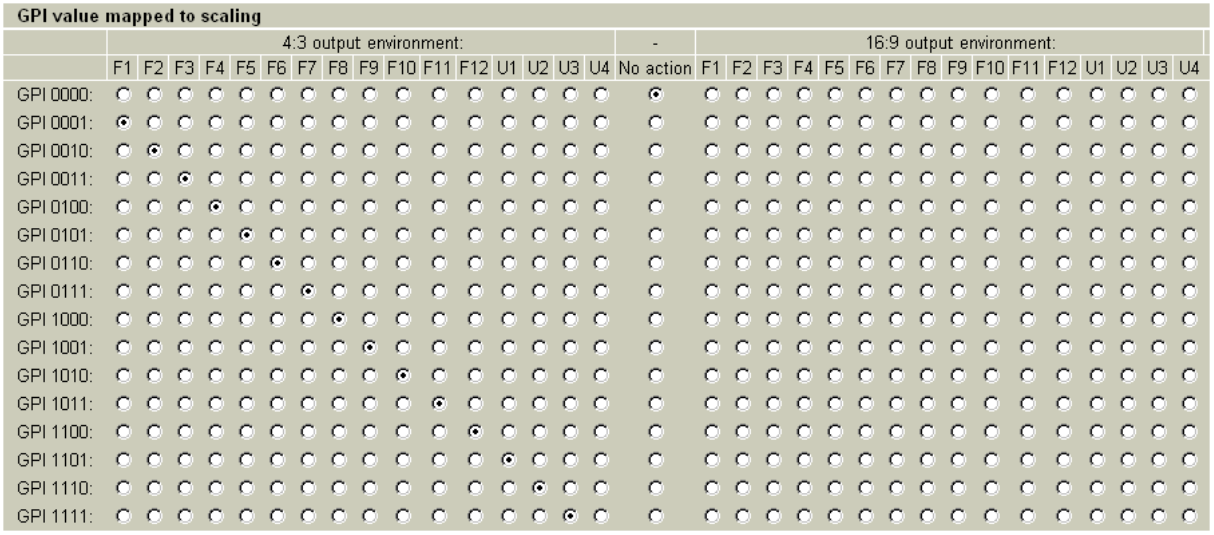
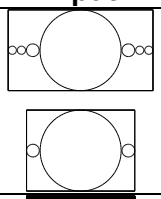
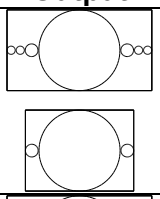
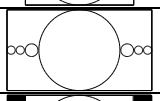
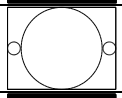
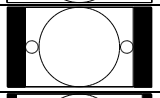
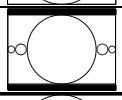
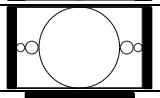
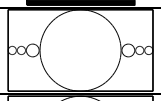
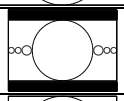
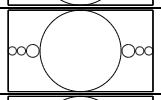
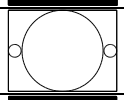
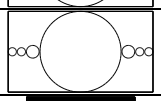
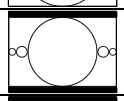
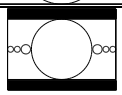
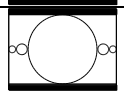
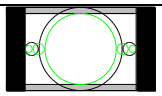
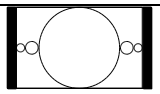
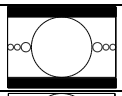
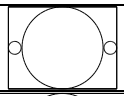
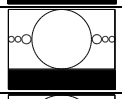
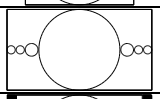
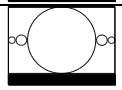
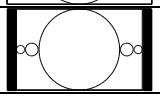



**Figure 3: Multicon GYDA view of the GPI to scaling map**

### 3.5.4 Pre-defined settings

| Input | Conversion | Output |
|---|---|---|
|  | No conversion |  |
|  | 4:3 cropped to 16:9 full frame |  |
|  | 4:3 to 16:9 with 4:3 pillar box |  |
|  | 4:3 cropped to 16:9 with 14:9 pillar box |  |
|  | 16:9 to 4:3 with 16:9 letterbox |  |
|  | 16:9 cropped to 4:3 full frame |  |
|  | 16:9 cropped to 4:3 with 14:9 letterbox |  |
|  | 4:3 with 16:9 letterbox cropped to 4:3 with 14:9 letterbox (zoom 1.143) |  |
|  | 16:9 with 4:3 pillarbox cropped to 16:9 with 14:9 pillarbox (zoom 1.167) |  |
|  | 4:3 with 16:9 letterbox cropped to 4:3 full frame (zoom 1.333) |  |
|  | Top 4:3 cropped to 16:9 full frame |  |
|  | Top 4:3 cropped to 16:9 with 14:9 pillarbox |  |

### 3.5.5 User defined settings

It is possible to set the scaling values and AFD output codes of four settings named “User scaling” 1 to 4. The scaling values control horizontal and vertical zoom, and horizontal and vertical center offset.

Vertical and horizontal zoom can be adjusted within the range 0.5 to 1.5. The values denote the enlargement of the output image.

Vertical and horizontal center offset values are slightly more complicated as the calculation depends on whether the active scaling zoom is greater of less than one.

**Zoom of one or less:**
The setting is in lines (vertical offset) and pixels (horizontal offset). A position value of P will result in the picture moving P pixels or lines.

**Zoom greater than 1:**
The setting is in lines (vertical offset) and pixels (horizontal offset) but the values are also scaled by the zoom factor. A zoom value larger than 1 with a position value of P will result in the picture moving (P x zoom) pixels or lines.

Positive position values moves image right/up, negative values left/down.

An AFD code may be embedded. Use the figure in the AFD conversion section to find the code that best describes the output picture.

## 3.6 Frame synchronizer

The frame synchronizer consists of a frame store buffer and some control logic. The frame store buffer can store up to 8 SD frames. The frame synchronizer is placed after the ARC block. The control logic sets the frame synchronizer either frame sync mode or frame delay mode of operation depending on the presence of the sync input signal.

If the sync input presence changes, the operational mode of the modules will change resulting in frame roll.

### 3.6.1 Frame Sync mode

If a sync input (B&B or Tri-level) is present, the module will output a signal that has a constant relative timing to this signal. Two parameters can be set; output phase and minimum delay.

The output phase can be positive or negative and sets the timing offset of the sync input and the video output.

The minimum delay sets the minimum delay between video output and video input. The actual delay can be larger than the minimum delay (hence the name), because the card must also adjust the picture phase relative to the sync input.

| The user may set the ‘minimum delay’ up to 7 frames. |
|---|

### 3.6.2 Frame delay mode

This mode is active when a sync signal is not present. The minimum delay setting is then used directly. 1 frame and 1 line minimum delay means that the output will be 1 frame and 1 line delayed version of the input.

## 3.7 Video generator

The video generator can produce one of the signals from the following list:-

- Color bar
- Checkfield
- Color bar with moving black box
- Black
- White
- Yellow
- Cyan
- Green
- Magenta
- Red
- Blue

The flat field option allows the user to specify any combination of luma and chroma values.

In normal operation (as a fallback generator), the video generator will take its video standard setting from the last video input seen by the board.

To enable the board to act as a standalone and user configurable video generator, the video generator must either be set as the first priority input when *Mode* is *auto*, or selected manually by setting *Mode* to *Video generator*. This will override any video input but the generator signal will still be locked to the sync or SDI inputs, if present. For true standalone generator operation, the inputs must be removed. Available video standards are 486/25i and 576/25i.

## 3.8 Label generator

The label generator consist of 2 lines of 16 characters each that are placed at the lower left corner of the active area.

Its main function enables the user to automatically add a label to the internal generator at loss of input signal. It is done by selecting the *auto* tick-box on the *Label generator* block in the Multicon GYDA configuration.

It is also possible to insert the label to the incoming SDI by ticking on the *Enable* tick-box.

> Note that to see the label on an output the video output selection must be set to "Processed" for that particular output.

## 3.9 Video processing block

The video processing block consists of a gain and offset adjustment, and a video payload legalizer.

### 3.9.1 Gain and offset

The gain and offset adjustment is done separately on the Y, Cb and Cr samples.

| | **Range Multicon GYDA** |
|---|---|
| Luma gain | 0 – 3.9999 |
| Chroma gain | 0 – 3.9999 |
| Luma offset (gain =1) | -511.75 – 511.75 |
| Chroma offset (gain = 1) | -255.75 – 255.75 |

### 3.9.2 Video payload legalizer

The legalizer hard clips the upper and lower limit of the video payload. With the legalizer enabled the limits are:

| | | |
|---|---|---|
| Upper limit | Luma: | 3ACh |
| | Chroma: | 3C0h |
| Lower limit | Luma: | 040h |
| | Chroma: | 040h |

With the legalizer disabled, the video processing block hard clips both luma and chroma to 3FBh and 004h.

## 3.10 EDH processing block

If enabled, the EDH processing block extracts the EDH packet from the video, updates the EDH flags according to SMPTE RP165 and inserts the EDH packet into the ancillary data of the video.

If disabled, The EDH processing block only reads, processes and reports the incoming EDH packet status and deletes the packet from the video stream.

## 3.11 Video output selection

The board has four outputs. They are organized in two pairs of inverting/non-inverting outputs. Each pair of outputs can be routed directly from the re-clocker or routed through the processing unit.

## 3.12 Audio overview

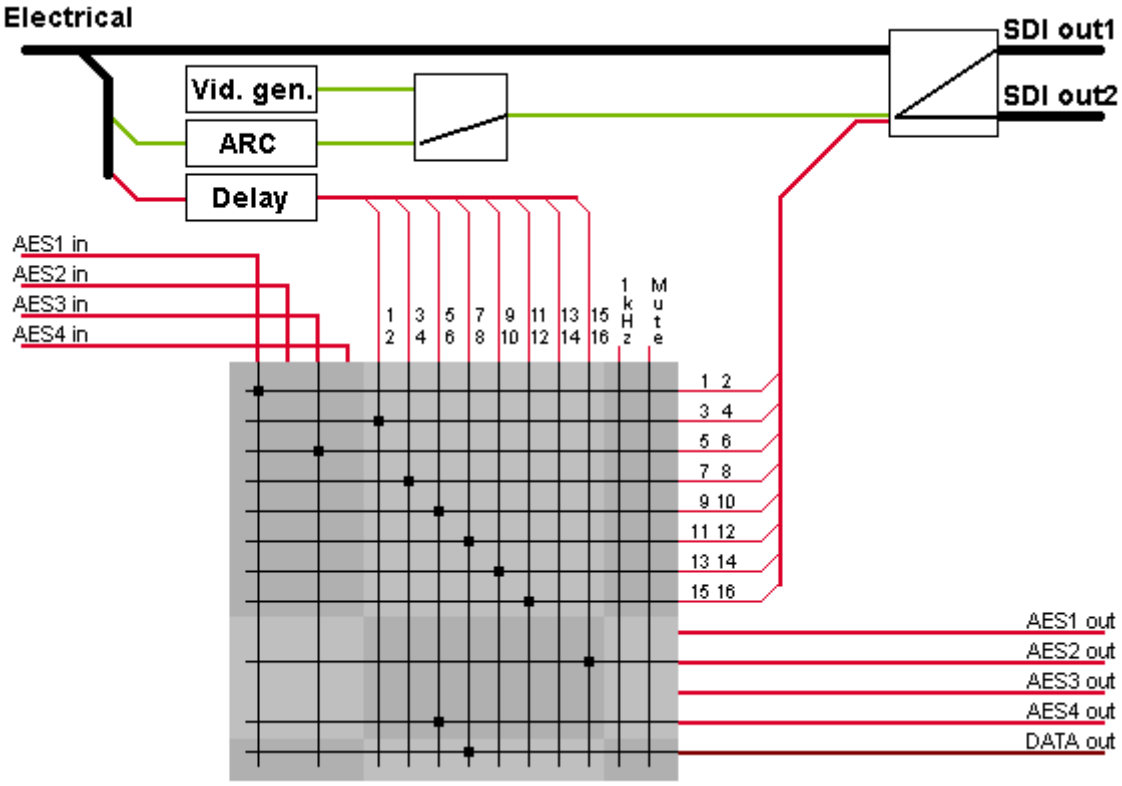



**Figure 4: Audio function blocks**

## 3.13 Audio de-embedder

The Audio de-embedder extracts all audio embedded in the video stream. The de-embedder is always enabled.

## 3.14 Audio delay

An audio delay can be specified relative to the video output. It is situated before the audio cross point matrix and is common for all de-embedded channels. The audio delay is specified in terms of 48 kHz audio samples, and can be set to positive or negative values.

*NOTE: As the audio delay is relative to the video output it is possible to specify an audio delay that will actually be a negative delay, i.e. ask that the sound is sent from the card before it is received. This will obviously cause audio errors.*

## 3.15 Audio cross point matrix

The audio cross point matrix is a 14x13 cross point with inputs and outputs as shown in Figure 4. The 8 de-embedded channels, a 1 kHz sine and “black sound” are selectable inputs. “Black sound” is explained in chapter 3.1. The outputs of the cross points are 8 stereo channels for re-embedding and one 4 AES output.

The 13 output channels from the cross point matrix have configurable fallbacks, used when their corresponding matrix inputs are missing. A common fallback setting is used for all eight re-embedder channels, whereas the 4 AES outputs have their own independent fallback settings. The priorities can be selected between *matrix* (being the selected channel in the cross point matrix) or the internally generated *sine* or *black sound.*

## 3.16 AES I/O

The direction of the four AES ports can be selected by the user. This means that the user has any combinations of inputs and outputs available: 4 inputs and 0 outputs, 3 inputs and 1 output, 2 inputs and 2 outputs, 1 input and 3 outputs or no inputs and 4 outputs.

### 3.16.1 Audio inputs

When an AES I/O port is set to be input, the sample frequency of the input is monitored to see if the signal is synchronous with the system clock. If not, the audio input is passed through a sample-rate converter. After the input block the audio can be delay with individual delay for each AES port, before it is routed to the audio matrix. The audio delay for AES inputs are set relative to the AES input port.

If the AES input port is synchronous with the SDI-input, the user can select the AES input delay to track to the video delay. The card will calculate the relative delay for the audio based on the delay setting for video and audio. This is useful if the SDI-in and AES has a common clock source and the sync input has a different clock source

### 3.16.2 Audio outputs

The AES outputs are routed from the audio matrix via individual audio processing blocks. The outputs are always 48 kHz and synchronous to the system clock. The AES outputs have individual fallback options.

## 3.17 Audio generator

The stereo audio generator is available as an input to the audio cross point matrix, and as a fallback option. There are therefore three slightly different ways to select the generator: select it in the matrix directly, select it as the first priority under audio fallback, or to set it as second priority behind a missing input.

The generator signal is a high purity 1 kHz sine wave with a 250ms interruption on the left channel every 3 seconds. The audio level may be set to one of two standards. The two levels are -18 dBFS and -20 dBFS. These two levels correspond to EBU R68 and SMPTE RP155.

## 3.18 Audio processing block

The output of each stereo signal from the audio cross point matrix may be processed in the audio processing block. This is controlled with the Multicon GYDA controller. The processing includes channel L/R manipulation and audio gain.

**Channel L/R manipulation**

The stereo signals may be output in one of the following ways:

| | |
|---|---|
| - LR, Left / Right | No change. |
| - RL, Right/ Left | Channels are swapped. |
| - LL, Left/ Left | Left channel is copied into the right channel. |
| - RR, Right/ Right | Right channel is copied into the left channel. |
| - !LR, ØLeft/ Right | The left channel is phase inverted. |
| - L!R, Left/ ØRight | The right channel is phase inverted. |
| - MM, (Left + Right)/2 | The left and right channels are summed. |
| - MS, MS/AB | The left and right channels are converted from AB stereo to MS stereo. |

The sum products (L+R/2 and MS) are reduced in level by 6 dB to avoid any possibility of clipping.

**Audio gain**
Audio gain is a 16 bit value that can be set for each stereo pair going into the audio processing block. The gain range is set to [+96dB, -96dB] with a gain step of 0.1dB.

Note that non-audio data is ignored and left unchanged by the gain function.

### 3.18.1 Audio embedder

The audio embedder can be enabled/disabled per group. When a group to be embedded is disabled the audio inside that group is removed.

A 24-bit audio signal uses the Extended Audio Data Packet for the 4 least significant bits. Not all equipment can handle Extended Audio Data Packets correctly, so the option exists to truncate all audio data to 20 bits. **This setting is common for all embedder channels.**

The insertion of Audio Control Packages can also be switched on and off. **This setting is also common for all embedder channels.**

# 4 Configuration

## 4.1 DIP switch functions

### 4.1.1 DIP switch functions

Note that the left DIP switch of the horizontal DIP package is number 1. The top DIP switch of the vertical DIP package is number 17.

| Switch # | Function name | Function DIPs | | | Comment |
|---|---|---|---|---|---|
| 1 | AES1 dir | Off = input<br>On = output | | | AES 1 input or output, if AES1 is input, DIP 2-4 routes GROUP 1. |
| 2-4 | AES1/GRP 1 routing | DIP 234 | Group 1 Embedding | AES1 output Deembedding | Routing matrix to AES1 or GROUP 1 |
| | | 000 | Disable | Group 1 ch 1&2 | |
| | | 001 | Group 1 | Group 1 ch 3&4 | |
| | | 010 | Group 2 | Group 2 ch 1&2 | |
| | | 011 | Group 3 | Group 2 ch 3&4 | |
| | | 100 | Group 4 | Group 3 ch 1&2 | |
| | | 101 | AES1&2 | Group 3 ch 3&4 | |
| | | 110 | AES3&4 | Group 4 ch 1&2 | |
| | | 111 | Generator | Group 4 ch 3&4 | |
| 5 | AES2 dir | Off = input<br>On = output | | | Aes 2 input or output |
| 6-8 | AES2/GRP2 | See table for AES1/GRP1 | | | Routing Matrix to AES2 or GROUP 2 |
| 9 | AES3 dir | Off = input<br>On = output | | | AES 3 in or out |
| 10-12 | AES3/GRP 3 | See table for AES1/GRP1 | | | Routing AES3 / GROUP 3 |
| 13 | AES4 dir | Off = input<br>On = output | | | AES 4 in or out |
| 14-16 | AES4/GRP 4 | See table for AES1/GRP1 | | | Routing matrix AES4 / GROUP 4 |
| X- Y | Frame delay | DIP[1 2] = [Off Off ] => 0 frms<br>DIP[1 2] = [Off Off ] => 1 frms<br>DIP[1 2] = [Off On ] => 2 frms<br>DIP[1 2] = [Off On ] => 3 frms | | | With a sync-input present, this sets the minimum frames delay.<br>Without a sync-input present this sets the no. of frames delay relative to the input. |

| | | | |
|---|---|---|---|
| ADLY | Audio follows video delay | On: De-embedded audio follows video. DIP 17-18 is used<br>Off: De-embedded audio will not use Frame delay from dip 17-18 | If on, de-embedded audio delay will follow video delay |
| OPT/EL | OPT/EL | | Optical / Electrical input |
| SDO1PROC | SDI OUT 1 | Off: through mode<br>On: processed mode | In through mode the video only goes through a re-clocker. |
| SDO2PROC | SDI OUT 2 | Off: through mode<br>On: processed mode | In through mode the video only goes through a re-clocker. |
| F-RESET | F-RESET | Off: Use values preset by MULTICON GYDA.<br>On: RESET to factory defaults | This DIP is only read at power up. After repowering with the DIP off, the board must be kept in the frame for minimum 10s to fully reset.<br>Values preset by MULTICON GYDA, are only values not set by DIPs, push buttons or rotary switches. |
| OVR | OVR | Off: MULTICON GYDA mode<br>On: Manual mode | This DIP is only read at power up.<br>OVR is short term for MULTICON GYDA override |

**Table 1: DIP SWITCH FUNCTIONS**

## 4.2 FACTORY reset function

A factory reset is a 3 step process:

1. Set DIP 15 to 'on' and boot the card (DIP 16 must also be set, or the other DIPs won't be read at all.)
2. Remove power and set the reset switch back to normal position ('off')
3. Power up the card as normal. The operation of the card will immediately reflect the freshly loaded default settings. However, the card must be kept powered for at least 10 seconds to ensure that these settings are stored locally to be retrieved again at the next start-up. The card's operational environment must also be kept static during those 10 seconds (i.e. no change in incoming video standard, no commands issued). Failing to meet these requirements could result in an incomplete reset and require the user to restart the factory reset sequence.

### 4.2.1 Rotary switch and push buttons

The *rotary switch*, labeled DLY, adjusts the phase delay from -5 to +4 video lines. It is only functional when a sync signal, black & burst or tri-level, is present at the sync input. The rotary switch is accessible from the board front.

The *push buttons,* labeled INC and DEC, are used to fine adjust the phase delay by samples. It can adjust ±½ video line for the current video standard (or the last video standard the board was able to lock to). Pressing a button and keeping it pressed will accelerate the change. The LED adjacent to the button will flash for a short period of time when the end of the adjustment range has been reached. Pressing both buttons at the same time will return to the middle of the adjustment range, and the board will acknowledge by flashing the INPUT and SYNC LEDs simultaneously.

## 4.3 MULTICON GYDA mode

All functions of the card can be controlled through the MULTICON GYDA control system. The MULTICON GYDA interface has an information page and a configuration page.

### 4.3.1 Information page

The information page shows a dynamic block-diagram of the board and some additional information text. The block diagram updates with the board status, showing selected input signal, missing signals (by red crosses over the appropriate signal lines) and signal routing (by graphic switches). It also shows the audio matrix selections that have been made in the configuration page.

> Note that if a stereo pair of embedded audio is missing, the user will still be allowed to select that pair from the audio matrix. The output will however go to the fallback position immediately. A missing stereo pair will be shown in the block-diagram as a red cross over the appropriate matrix input line.

The text on the information page gives information about functionality not displayed on the dynamic block diagram.

The video delay represents the actual delay between input and output video.

Embedded UART shows the data rate of the data link embedded in the audio control packages on the incoming signal.

### 4.3.2 Configuration page

The different configuration possibilities are explained in Chapter 3, under the corresponding blocks or functions.

# 5 Connections

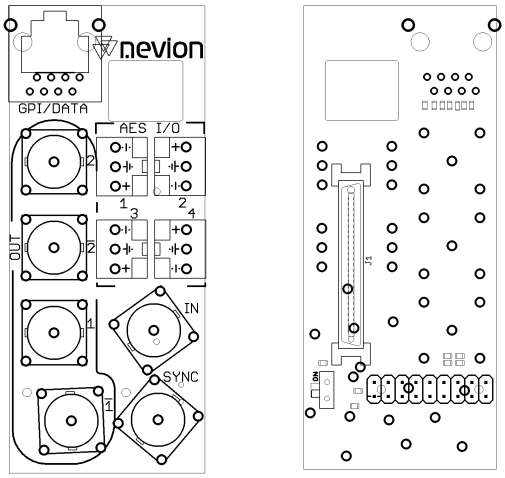
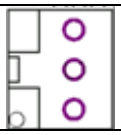
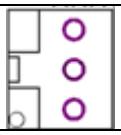
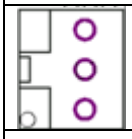
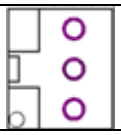



**Figure 5: ARC-SD-XMUX4-R backplane**

The backplane for the ARC-SD-XMUX4 is called FRS-HD-XMUX4-C1. The table below shows the connectors and their functions.

| Function | Label | Connector type |
|---|---|---|
| SD-SDI input | IN | BNC |
| SD-SDI output 1 | 1 | BNC |
| SD-SDI output 1 inverted | $\overline{1}$ | BNC |
| SD-SDI output 2 | 2 | BNC |
| SD-SDI output 2 inverted | $\overline{2}$ | BNC |
| Black & Burst/ tri-level input | SYNC | BNC |
| AES I/O 1 | AES | WECO Audio connector<br>  <br>Positive<br>GND<br>Negative |
| AES I/O 2 | AES | WECO Audio connector<br>  <br>Positive<br>GND<br>Negative |
| AES I/O 3 | AES | WECO Audio connector<br>  <br>Positive<br>GND<br>Negative |
| AES I/O 4 | AES | WECO Audio connector<br>  <br>Positive<br>GND<br>Negative |
| GPI in | GPI/DATA | TP45, pin 2, 3, 6 & 7 |
| GPI out | GPI/DATA | TP45 pin 1 (pin 8 = GND) |
| DATA out | GPI/DATA | TP45 pin 4 & 5 |
| Optical input | OPT1 | BSC-II (for SC input) |

# 6 Operation

## 6.1 Front panel LED indicators

| Diode \ state | Red LED | Orange LED | Green LED | No light |
|---|---|---|---|---|
| **Card status** | PTC fuse has been triggered or FPGA loading has failed | FPGA loading. If constantly lit for more than a few seconds: DIPs 14+15 both set to the 'On' position, or module not programmed | Module is OK | Module has no power |
| **SDI input status** | Video signal absent | Video signal present but card not able to lock VCXO | Video input signal in lock | Module not programmed, or DIPs 14+15 both set to the 'On' position |
| **Sync input status** | Sync signal absent | Sync signal present but card unable to lock VCXO | B&B or Tri-level sync in lock | Module not programmed, or DIPs 14+15 both set to the 'On' position |
| **Audio input status** | No audio embedded in incoming video | One, two or three audio groups embedded in incoming video | 4 audio groups embedded in incoming video | Module not programmed, or DIPs 14+15 both set to the 'On' position |

Note that three special conditions also exist:

When all four LEDs blink synchronously, this is the result of a *locate on* command. This condition will eventually time out, but can also be reverted by issuing the *locate off* command.

The second special condition is when an FPGA firmware upgrade is performed: When Multicon GYDA is finished transferring the compressed data file, the card will spend some time unpacking this file and during this time it will not respond to commands or update settings. During this time it will display running lights (three LEDs lit, one dark, the position of the dark LED will move around).

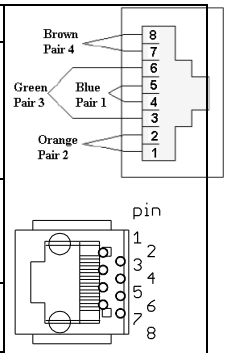
The last special condition is when the user adjusts the phase delay with the push buttons at the front of the card. Short flashes on the SYNC *or* INPUT LEDs means that the end of the adjustment range has been reached. If they flash simultaneously, both push buttons have been pressed simultaneously and the samples part of the phase delay reset to the middle of the adjustment range.

## 6.2 GPI alarms

The UDC-HD-XMUX4 has one GPI output. This reflects the status of the card, see the table below.

### 6.2.1 Functions of 8pin modular jack

| GPI name | Function | Pin # | Mode | Direction |
|---|---|---|---|---|
| Status | General error status for the module. Will also activate at firmware upgrades. | Pin 1 | Inverted Open Collector (open is alarm) | Output |
| GPI 1 | GPI default scaling select. Least significant bit. | Pin 2 | TTL, 0V = active level | Input |
| GPI 2 | GPI default scaling select | Pin 3 | TTL, 0V = active level | Input |
| DATA-link output | RS422+ | Pin 4 | RS422 | Output |
| DATA-link output | RS422- | Pin 5 | RS422 | Output |
| GPI 4 | GPI default scaling select. Most significant bit. | Pin 6 | TTL, 0V = active level | Input |
| GPI 3 | GPI default scaling select. | Pin 7 | TTL, 0V = active level | Input |
| Ground | 0 volt pin | Pin 8 | 0V. | |




## 6.3 RS422 commands

### 6.3.1 FLP4.0 required commands

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| - | - | ? | ? | *product name*\<br>SW rev *n.m*\<br>FW rev *r.s*\<br>protocol ver 4.0\ | ***Hello* command**.<br>*Note 1: No other commands will be available until the card has received this hello.*<br>*Note 2: This command will also enable checksums.*<br>*Note 3: Cards are designed to be hot-swappable. To sync with the start of a new command, the cards will wait for a <lf> character before looking for a valid command.* |
| conf | 0 | - | conf 0 | *too long to list* | **Configuration settings**<br>Retrieves the card's configurable settings. Each addressable block is represented by a single line. Dynamic status *may* be included in response, but is usually reported in *info* only. |
| - | - | info | info | *too long to list* | **Dynamic status info**<br>Blocks with static settings only will usually not be included, see *conf* above. |

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| - | - | chk off | chk off | ok | **Checksum off**<br>If issued twice in succession, this command will disable checksums. Note: Responses will still have the checksums appended.<br>*NOTE1:? command turns the checksum on again* |
| - | - | locate on <seconds><br><br>locate off | locate on 3<br><br>locate off | ok | **Card locator**<br>This command will cause all the LEDs to flash for a user specified number of seconds. If omitted, the value <seconds> will be set to a default of 120 seconds. The flashing can be terminated at any time with *locate off*. |
| - | - | address | address | address <address> | **Card address**<br>This command will force the module to check and update its current rack and slot address. This is normally only done at start-up. |
| - | - | filename | filename arcsddmux-0-101.ffw | <name>'.'<extension> | **Firmware update**<br>The <name> part must match the card's hardware and include a revision number, and the extension must be either 'ffw' for FPGA firmware or 'mfw' for microcontroller firmware. After running this command the board will be ready to receive its new firmware. |
| - | - | fin | Fin | ok | **Finalize**<br>Finalize the programming of the microcontroller. See description of the uC boot loader (separate document). |
| misc | 0 | - | STATUS NOT AVAILABLE BY COMMAND,<br>ONLY FOUND in *conf 0* AND *info* RESPONSES! | prog \| fin<br><br>' ' \| ovr | **Misc info**<br>*prog* if the card is freshly programmed by the boot loader and the program is still un-finalized. *fin* is the normal condition.<br>*ovr* if DIP-switch 16 is set to the ON position and the card is under DIP-switch control.<br>Note 1: The info part of misc has additional functionality when locate is used: *locating <remaining seconds>.* This enables a visible countdown clock in Multicon GYDA, but is not a required part of FLP400. |

### 6.3.2 Normal control blocks

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| ablk | 0-3 | dir in \| out<br>track none \| video | ablk 0 dir in<br>ablk 0 track video | dir in \| out<br>track video \| none | **AES I/O port 1-4**<br>dir in \| out sets the direction of the AES I/O.<br>track selects whether AES delay tracks the video delay. |
| agen | 0 | lvl <sine_level>cBFS | agen 0 lvl -180<br>agen 0 lvl -200 | sine 1kHz lvl <sine_level>cBFS | **Audio generator**<br>The amplitude of the generated sine that can be chosen as fallback in audio change-overs. Legal values are -180cBFS or -200cBFS (centiBel referred to full scale output). Units are optional, but if included must be written as cBFS (case sensitive). |
| aprc | 0-11 | lr \|<br>rl \|<br>ll \|<br>rr \|<br>nlr \|<br>lnr \|<br>mm \|<br>ms \|<br>lvl <gain> | aprc 0 lr<br>aprc 3 ll<br>aprc 6 mm<br>aprc 7 lvl -400 | lr \|<br>rl \|<br>ll \|<br>rr \|<br>nlr \|<br>lnr \|<br>mm \|<br>ms | **Audio processing**<br>one block for each output from cho 2-13. The meaning of the commands are as follows:<br>lr = Normal<br>rl = Channel swapped<br>ll = Left channel to both output channels<br>rr = Right channel to both output channels<br>nlr = Left channel phase inverted<br>lnr = Right channel phase inverted<br>mm = Mono, both channels = (r+l)/2<br>ms = Mono/stereo, m=(l+r)/2, s=(l-r)/2<br>lvl means level and is the gain setting. |
| ceq | 0 | - | ceq 0 | cd \| ncd | **Cable equalizer** for electrical input. No control; only used to report *carrier detected* or *no carrier detected.* |
| cho | 0 | pri <k> \|<br>pri <k> <l> \|<br>pri <k> <l> <m><br><br>pos man <k> \|<br>pos auto<br><br>latch reset<br><br>t1 <hold_time><br><br>t2 <lock_time> | cho 0 pri 0<br>cho pri 0 1<br>cho pri 10 2<br><br>cho 0 pos man 1<br>cho 0 pos auto<br><br>cho 0 latch reset<br><br>cho 0 t1 1000<br><br>cho 0 t2 1000 | size 3 pri *k*,*l*,*m* auto t1 <hold time> t2 <lock time><br><br>size 5 pri *k*,*l*,*m* man *m* latch t1 <hold time> t2 <lock time> | **Video input select**<br><br>***pri*:** a prioritized list of inputs, used when change-over is automatic. The list can have 1, 2 or 3 entries, or *levels*. Manual mode is effectively the same as automatic mode with one priority level only, but has its own command.<br>0 = from electrical input<br>1 = from optical input<br>2 = internal video generator<br>3 = mute<br>4 = none<br><br>The module will always respond with 3 levels, filling in 4=none for the levels not used.<br><br>***t1* and *t2*:** change-over doesn't happen immediately, as a precaution against glitches and unstable signals. The timers t1 and t2 let the user decide how long (in ms) we will cling on to a missing input before we consider it gone and move on to the next pri level, and how long an input with a higher priority should be present before we consider it |

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| | | | | | repaired and switch back, respectively. |
| cho | 1 | | | size 3 pri *k*,*l* auto<br><br>size 3 pri *k*,*l* man *m* | No commands available. Included to show internal status and to update Multicon GYDA graphics. |
| cho | 2-13 | pri <k> \|<br>pri <k> <l> | cho 2 pri 1<br>cho 5 pri 0 2 | size 4 pri *k*,*l* | **Audio fallback setting**<br>Audio change-over blocks, one cho per audio output from the audio matrix, mtx 0. No other settings but the priority list.<br>0 = from audio matrix<br>1 = sine<br>2 = AES with silence<br>3 = mute<br>*Note: Only generators (pri 1, 2 or 3) are allowed to be set as first and only priority.* |
| cho | 14 | pri <k> \|<br>pri <k> <l> | cho 12 pri 1<br>cho 12 pri 0 2 | size 4 pri *k*,*l* | **Embedded audio common fallback setting**<br>A short-cut to set change-overs 2-9 all at once. Will of course not report anything in info, that's left to the individual cho blocks. |
| demb | 0-3 | - | demb 0<br>demb 2 | grp *k* en | **Audio de-embedders**<br>one permanently assigned to each incoming group, always enabled. No control available. |
| dly | 0 | <frames>frms | dly 0 2frms | 'tgt' <frames> frms | **Video delay**<br>This sets the additional video delay of the card.<br>In info this block reports back the current delay in nanoseconds. This will vary with the incoming video standard. |
| dly | 1 | <audio_samples>sps | dly 1 -30sps | 'tgt' <audio_samples> sps | **audio delay for deembedded audio**<br>The audio delay is given in audio samples. Audio delay is always given relative to video. |
| dly | 2 | <audio_samples>sps | dly 1 -30sps | 'tgt' <audio_samples> sps | **audio delay for input AES 1**<br>The audio delay is given in audio samples. Audio delay is always given relative to input AES 1. |
| dly | 3 | <audio_samples>sps | dly 1 -30sps | 'tgt' <audio_samples> sps | **audio delay for input AES 2**<br>The audio delay is given in audio samples. Audio delay is always given relative to input AES 2. |
| dly | 4 | <audio_samples>sps | dly 1 -30sps | 'tgt' <audio_samples> sps | **audio delay for input AES 3**<br>The audio delay is given in audio samples. Audio delay is always given relative to input AES 3. |
| dly | 5 | <audio_samples>sps | dly 1 -30sps | 'tgt' <audio_samples> sps | **audio delay for input AES 4**<br>The audio delay is given in audio samples. Audio delay is always given relative to input AES 4. |
| dly | 6 | <lines>lines <samples>sps | dly 2 1lines -30sps | 'phase' <lines> lines <samples> sps | **Video phase**<br>If lines != 0 the resulting phase will vary with incoming video standard, see dly 0 above. |

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| emb | 0-3 | en \| dis<br><br>acp ( on \| off )<br><br>use24 ( on \| off )<br><br>del (off \| (on <del12> <del34>)) | emb 0 en<br>emb 2 dis<br>emb 1 acp on<br>emb 3 acp off<br>emb 1 use24 on<br>emb 2 use24 off<br><br>emb 0 del off<br>emb 2 del on 54 -432 | (en \| dis) use24 (on \| off) acp (on \| off) del (off \| (on <del12> <del34>)) | **Audio embedder block**<br>**en/dis:** Enables or disables the embedding of the group into the ancillary area.<br><br>**acp on/off:** This is valid only for SD and enables the audio control package.<br><br>**use24 on/off:** This is only valid for SD and selects between 24bit and 20bit sound.<br><br>**del off/on delay12 delay34:** For each of the embedder groups the delay bits for ch1+2 and for ch3+4 can be inserted into the ACP. The delay value can be positive and negative and is put directly into the ACP as it is written.<br>*Note: To set both delays to 0 would be the same as turning the delays off. The response reflects this.* |
| gpi | 0 | act \|<br>inact | gpi 0 act<br>gpi 0 inact | gpi 0 act id “EDH generator”<br>gpi 0 inact id “EDH generator” | **EDH insert select**<br>This gpi works as a simple 2:1 switch.<br>inact : EDH off<br>act : EDH on |
| mtx | 0 | <i1> <o1> ...<iN> <oN><br><i1> <o1>,<o2>,...<oN><br><i1> <o1> - <o2><br><br>..or the above combined | mtx 0 0 2 1 4 5 5<br>mtx 0 0 0, 1 1, 2 2<br>mtx 0 0 0-9<br><br>mtx 0 0 0 1 1 2 2-9 | size M:N i1 i2 i3... iN | **Audio matrix**<br>mtx 0 (size 10:10) controls the audio matrix; outputs 0-7 are embedded sound, 8=adac and 9=AES.<br>*Note: Any combination of the three basic commands are allowed, for instance the following command to set up a 10x10 audio matrix in a single line:*<br>*mtx 3 1 1 2 2 3 0,3-9*<br>*=> mtx 3 size 10:10 3 1 2 3 3 3 3 3 3* |
| mtx | 1 | <i1> <o1> ...<i2> <o2><br><i1> <o1>,<o2> | mtx 1 0 0 1 1<br>mtx 1 0 0,1 | size M:N i1 i2 i3... iN | **Video output matrix**<br>mtx 1 (size 2:2) controls the video output switches.<br>0: Through mode (re-clocked only)<br>1: Processed mode (SDI from FPGA) |
| mtx | 2 | | mtx 2 0 1 | mtx 2 size 2:1 1 | **Embedder enable**<br>Has no effect in this product. |
| mtx | 3 | | mtx 3 10 0<br>mtx 3 1 0<br>mtx 3 0 0 | mtx 3 size 16:1 10<br>mtx 3 size 16:1 1<br>mtx 3 size 16:1 0 | **Deafult scaler matrix**<br>mtx 3 (size 16:1) controls scaling to use when default scaling is selected. |
| mtx | 4 | | mtx 4 10 0 | mtx 4 size 17:16 10 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 | **GPIs mapped to scalings**<br>mtx 4 (size 17:16) controls how the 4-bit GPI values are mapped to the 16 available scalings. The 12 fixed scalings are 0-11, the 4 user scalings are 12-15. The 17th option is to not perform any action |
| mtx | 5 | | mtx 5 | mtx 5 size 37:1 10 | **Active scaling**<br>mtx 5 (size 16:1) tells which scaling is currently used. No commands |

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| | | | | | available. |
| pin | 0 | on \| off | pin 0 on<br>pin 0 off | cd \| ncd | **Pin diode for optical input**. No control available, except to turn power to the pin diode on or off. The info string reports *carrier detected* or *no carrier detected.* |
| rcl | 0 | - | rcl 0 | lock \| lol | **Reclocker**. No control; only used to report *lock status.* |
| scale | 0-11 | out env (16/9 \| 4/3)<br><br>out afd <afd-code> | scale 0 out asp 16/9<br>scale 0 out asp 4/3<br>scale 0 out afd 8<br>scale 0 out afd 11 | out zoom <Hscale> <Vscale> pos <Hpos> <Vpos> env ( 16/9 \| 4/3 ) afd <AFD-code> | **Premade scale blocks.**<br>12 fixed scale settings. The user can only change output environment and output afd-code. |
| scale | 12-15 | out zoom <Hzoom> <Vzoom><br>out pos <Hpos> <Vpos><br><br>out env (16/9 \| 4/3)<br><br>out afd <AFD-code> | scale 12 out zoom 1.33 1.33<br>scale 12 out pos 0.002 0.002<br><br>scale 12 out env 16/9<br>scale 12 out env 4/3<br><br>scale 12 out afd 8<br>scale 12 out afd 11 | out zoom <Hscale> <Vscale> pos <Hpos> <Vpos> env ( 16/9 \| 4/3 ) afd <AFD-code> | **User scale blocks.**<br>Four user scale settings.<br>**Zoom:**<br>Zoom range is from 0.5 to 1.5.<br>**Position:**<br>Position when zoom is < 0 defines where in the output frame the box is placed. The box will never move outside of the frame.<br><br>When zoom is > 0 the position defines which part of the input picture to use.<br><br>A value of 0 is center. Positive values moves picture to the right or up. Negative values moves picture to the left or down. |
| scale | 16 | out env (16/9 \| 4/3)<br><br>out fill ( full \| crop \| 14/9 )<br>rule <rule-value><br><br>ins <insert-value> | scale 16 out env 16/9<br><br>scale 16 out fill full rule 0x02<br><br><br>insert 0x20 | scale 16 out env 16/9 fill full rule 0x1 use 0xF ins 0x20 use 0x3E | **Master scale control block**<br>This block sets the conversion mode of the card and what aspect ratio information will be inserted in the output video.<br><br>**Output environment:**<br>out env can be 16/9 or 4/3. This controls the pixel aspect ratio of the output video.<br><br>**Fill:**<br>Fill selects how much of the picture is preserved.<br>full: protect input frame<br>crop: zoom to fill frame<br>14:9: scale to 14:9 PB or LB<br><br>**Rule:**<br><rule-value> can take on the following values, and tells the card which incoming aspect ratio information to use:<br>0x01: AFD -> Fill -> Default<br>0x02: AFD -> Default<br>0x04: Fill -> Default<br>0x08: Default<br>No other values will be accepted by the card, no combinations are available. |

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| | | | | | **Insert:**<br>The <insert -value> can be any binary combination of the following values:<br>0x02: WSS Extended<br>0x04: WSS<br>0x08: SMPTE352<br>0x10: Video Index<br>0x20: AFD<br>Note that the value 0x01 is not currently supported, and that the card therefore will only accept even numbers as <insert-values>. |
| supr | 0 | ( en \| dis \| auto )<br>font <font><br><br>lb <label_page><br><ASCII00><br><ASCII01> …<br><ASCII15> | supr 0 auto<br>supr 0 font 0x4e4<br>supr 0 size 10<br><br>supr 0 lb 0 65 66 67 0 | supr 0 font 0x4e4 lb 0 65 66 67 0 | **Video label**<br>The video label is a text string that is superimposed on the video. This feature can be enabled (en) at all times, disabled (dis) at all times, or enabled only when the internal video generator is active (auto).<br>Maximum string length is 32 characters, over maximum 2 lines. The linefeed character (ASCII 10) is counted as one character, leaving 31. Strings can be terminated at any time using ASCII 0. There's an implicit ASCII 0 on the 33rd character place. The example string on the left will display 'ABC' on a single line.<br>The 32 characters are transmitted in two pages of 16 characters each. These pages are prefixed 'lb 0' and 'lb 1'. |
| sync | 0 | - | sync 0 | lol \| ( lock ( rilvl \| bb \| sdi ) ) | **Sync block**<br>Frequency reference for video output. Status only, no commands available. |
| uart | 0 | - | | tx | **The embedded data link**, selectable by cho 13. No control possible, the word tx indicates that this is a transceiver only.<br>Uart info reports link status: *los* (loss of signal), *raw*, or the speed of the embedded link (example: *115200/8/n/1*). |
| vgen | 0 | cbar \|<br>chkfield \|<br>white \|<br>yellow \|<br>cyan \|<br>green \|<br>magenta \|<br>red \|<br>blue \|<br>black \|<br>mcbar<br><br>flat <Y> <Cb> <Cr><br><br>video <lns>/<rate><scan> wss (off \| (on <wss_val>) ) | vgen 0 cbar<br><br><br><br><br>vgen 0 flat 200 0 100<br>vgen 0 video 576/25i<br>vgen 0 video 486/29i<br><br>vgen 0 wss auto<br>vgen 0 wss on 7 | video <lns>/<rate><scan> wss ( auto\| off \| ( on <wss_value> ) ) (cbar \| chkfield \| white \| yellow \| cyan \| green \| magenta \| red \| blue \| black \| mcbar \| (flat <Y> <Cb> <Cr>) ) | **Internal video generator.**<br>The video generator will be activated in two different ways: If selected as a fallback option the generator will generate the selected pattern when the other input(s) are missing, and then use the video settings from the last external source present. It can also be selected as the main input in cho 1, in which case its own video settings will also be used. cbar denotes colorbar, while mcbar denotes colorbar with an superimposed moving black box. |

| Block | Blk # | Commands | Example | Response | Control |
|---|---|---|---|---|---|
| vmon | 0 | msk <16b_mask><br><br>reset | vmon 0 msk 0xFFFF<br><br>vmon 0 reset | msk <16b_mask> | **Video monitoring.**<br>Error counting. The count itself is reported in info. Errors can be masked off and not counted; this is the purpose of the mask. The counter itself is 16b and will wrap around, but can also be reset by issuing *reset*. |
| vprc | 0 | lglz on \|<br>lglz off<br><br>(y \| cb \| cr) <gain> <offset> | vprc 0 lglz on<br>vprc 0 lglz off<br>vprc 0 y 1.03 4.0<br>vprc 0 cb 0.96 0.0<br>vprc 0 cr 1.34 -3.23 | lglz ( on \| off ) y <ygain> <yoffset><br>cb <cbgain> <cboffset><br>cr <crgain> <croffset> | **Video processing block**<br>Gain and offset must be given as floating point numbers. Gain is limited to [0, 4> for luma and chroma, while offsets are limited to <-1024, 1024> for luma and <-512, 512> for chroma. |

### 6.3.3 Commands intended for debug/lab use only

| Block | Blk # | Commands | example | Response | Control |
|---|---|---|---|---|---|
| spi | - | on \| off | spi on<br>spi off | | spi off used to isolate the uC from the SPI lines during programming of the flash by external programmer. spi on must be issued in order to re-enable normal card operation with the uC as the SPI master. |
| spir | - | <address> | spir 0x0004 | | Read a single word (or byte) from a SPI registers. Addressing is 16b and most significant nibble determines which chip. These are the address ranges:<br>0x0000 – 0x0fff : AES dir and SRC<br>0x1000 – 0x1fff : FPGA<br>0x2000 – 0x2fff : flash<br>0x3000 – 0x3fff : deserializer<br>0x4000 – 0x4fff : serializer<br>0x5000 – 0x5fff : shift register for LEDs<br>0x6000 – 0x6fff : F-RAM<br>0x7000 – 0x7fff : Rotary switches |
| spiw | - | <address> <data> | spiw 0x0004 0x2c | | With the same address ranges as for spir above, this command allows the user to modify SPI registers. |
| thebug | - | - | thebug | | A collection of debug information that is presented in a Multicon GYDA block-like format. First line tells which image is currently loaded. Second line contains the filename and version of the uC software, including the AVR controller it was compiled for. The third line contains the SW flags in uC, the number of times the watchdog timer has kicked in, readout of dip-switches, input select for deserializer, SDOn on/off, slew rates, and status for the video changeovers.<br>The next two lines contain raster information from the deserializer and serializer respectively, while the next two lines contain sample values for mlines and VCXO. |

# General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
   - Operating room temperature range: 0°C to 45°C
   - Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:
   - Temperature range: -10°C to 55°C
   - Relative humidity range: <95% (non-condensing)

## Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

# Appendix A Materials declaration and recycling information

## A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the “Administrative Measure on the Control of Pollution by Electronic Information Products”. In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

| 組成名稱<br>Part Name | Toxic or hazardous substances and elements | | | | | |
|---|---|---|---|---|---|---|
| | 鉛<br>Lead (Pb) | 汞<br>Mercury (Hg) | 镉<br>Cadmium (Cd) | 六价铬<br>Hexavalent Chromium (Cr(VI)) | 多溴联苯<br>Polybrominated biphenyls (PBB) | 多溴二苯醚<br>Polybrominated diphenyl ethers (PBDE) |
| ARC-SD-XMUX4 | O | O | O | O | O | O |
| O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.<br><br>X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006. | | | | | | |

This is indicated by the product marking:

## A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site http://www.nevion.com/. Please contact Nevion’s Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.