



ARC-SD-DMUX ARC-SD-DMUX-R

SD-SDI Aspect Ratio Converter
with Audio De-embedding

User manual

Rev. B

A large, solid green circular graphic with a white circular cutout in the center, located in the bottom right corner of the page.

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Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
B	1	2013-10-29	TB	Corrected bit depth for analog video; new template
1	A	2010-03-09	MDH	Editing release
A	-	2009-10-05	JD	First preliminary release

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1 Product overview

The Flashlink ARC-SD-DMUX converts the aspect ratio of a SD-SDI signal. The module changes the scaling during the vertical blanking period so that the changes are apparently instantaneous.

Two SDI outputs and a set of configurable analog video outputs are provided.

The ARC-SD-DMUX is also a frame synchronizer with an adjustable offset relative to the sync signal.

The ARC-SD-DMUX also has a de-glitcher to give error-free synchronous switching.

The audio embedded in the SD-SDI stream is de-embedded and can be delayed relative to video. The stereo audio channels can be swapped in the audio matrix before they are re-embedded in the SD-SDI data output stream.

A selection of user parameters of the card can be controlled by switches on the board. Complete control of all parameters is available by use of the Flashlink RS422 Control Protocol Version 4, which is supported by the Multicon GYDA system controller from software release 2.13.

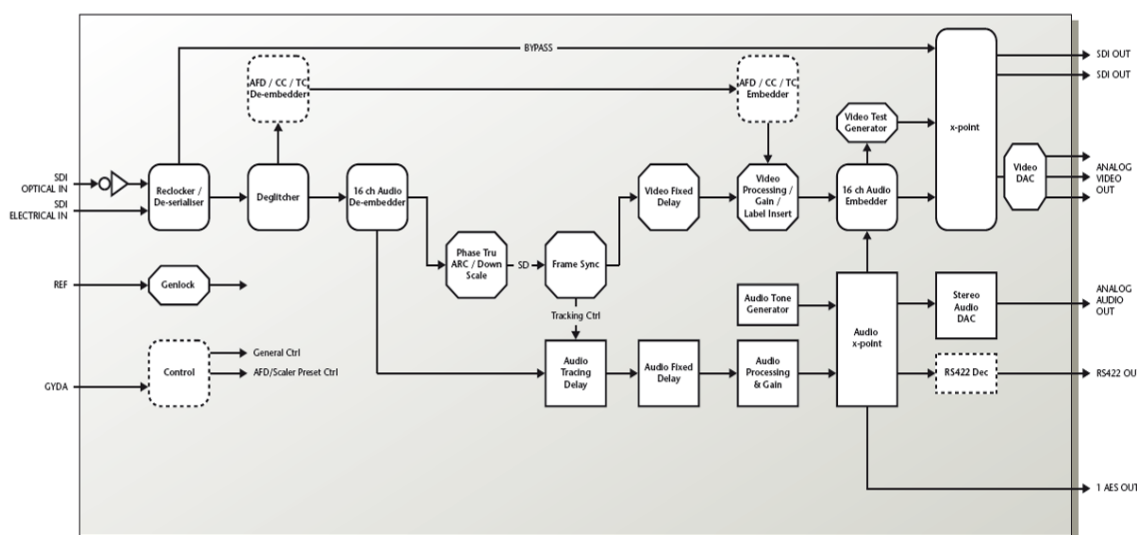


Figure 1: ARC-SD-DMUX-R block diagram

1.1 Product versions

ARC-SD-DMUX

SD-SDI aspect ratio converter. With 2XSD-SDI out, analog video outputs, internal audio handling, analog audio outputs, AES (or RS-422 data) out, and frame synchronizer functionality.

ARC-SD-DMUX-R

As above with the addition of a high sensitivity 9/125µm single mode optical input.

2 Specifications

2.1.1.1 Optical SD-SDI input

Data rate:	270 Mbps
Sensitivity:	Better than -22dBm
Detector overload threshold:	-3dBm
Detector damage threshold:	>+1dBm
Optical wavelength:	1200-1620nm
Transmission circuit fiber:	9/125um Single Mode
Return loss:	>27dB
Connector:	SC/UPC

2.1.1.2 Electrical SD-SDI input

Connectors	75 Ohm BNC
Equalization	Automatic: <ul style="list-style-type: none"> - >300m @270Mbps w/Belden 8281, BER < 10E-12
Input Return loss	>15dB, 5MHz -270MHz
Jitter tolerance	- SD limit: <ul style="list-style-type: none"> - 10Hz-1kHz: >1 UI - 10kHz – 5MHz: >0.2 UI

2.1.1.3 Electrical Sync input

Connector	75 Ohm BNC
Format	Black & Burst, Tri-level
Input Return loss	<-35dB @ < 10MHz, 30dB @ < 30MHz

2.1.1.4 Electrical SD-SDI outputs

Number of outputs	2
Polarity	Non-inverting
Connectors	75 Ohm BNC
Output Return loss	>15dB, 5MHz -270MHz
Output signal level	800mV +/- 10%
Output signal rise / fall time, 20% - 80%	- SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var.
Amplitude overshoot	<10%
Output timing jitter	- SD: <0.2 UI
Output alignment jitter	- SD: <0.15 UI

2.1.1.5 Analog Video outputs

Number of outputs	1 Component YUV or 3 CVBS
Connector	3 x 75R BNC
DC offset	< 0±15mV
White level, NTSC	100±1 IRE
Sync level, NTSC	40±1 IRE
Return loss	> 35dB @ 10MHz, >40dB @ 5MHz
White level, PAL	100±1 IRE
Sync level, PAL	40±1 IRE
Diff gain	<0.5%
Diff phase	<1deg
AM noise	< -60dB
PM noise	< -60dB
S/N	< -60dB
2T K-factor	< 0.5%
(2T pulse distortion)	
Luma non-linearity	< 2%
Output resolution	12 bits

2.1.1.6 Analog Audio output

Number of outputs	1 stereo pair
Connectors	2 x WECO audio connectors
Impedance	< 66ohm
Dynamic range	>100dB(A)
Crosstalk	< -60dB 20Hz-20kHz
THD+N	Better than 0.03%
Frequency response	20Hz-20kHz +/- 0.5dB
Output level	24dBu +/- 1dB
Common mode DC	0 to +50V
Immunity	
Level adjustment range	0 – 24dBu with 1dB step
Two tone intermodulation	< -80dB
Output resolution	24 bits

2.1.1.7 AES output

Number of outputs	1
Connectors	WECO audio connector
Return loss	110R +/-20% 0.1MHz – 6.144MHz
Output jitter	<0.0025UI peak

2.1.1.8 Supported standards

SD, 270 Mbps	SMPTE 259M, SMPTE 272M-AC, SMPTE297M
Analog video	SMPTE 170M, SMPTE 274M, ITU-R. BT.470,
Centre of picture definition	SMPTE RP187, ITU-R. BT.470
Aspect ratio preservation	SMPTE RP199-1999, SMPTE RP221
Video switch point definition and sync	SMPTE RP168 (tri-level), SMPTE 170M, ITU-R. BT.470
AES	AES3-1996
Optical	SMPTE 297M
EDH	Compliant to SMPTE RP165
Video Payload Identification	SMPTE 352M-2002, SMPTE 2016-1, SMPTE 2016-3, SMPTE RP 186

2.1.1.9 Minimum video signal delay through processing

Minimum delay	256 lines
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2.1.1.10 Other

Power consumption	+5V DC/ 4.6W (4.2W without optical receiver) +15V DC / 2.55W -15V DC/ 0.5W
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Max 6 cards per frame with dual PWR-AC-75W

3 Description

3.1 Data paths

The SD-SDI input selected from the optical or electrical input is equalized, re-clocked and de-serialized and transferred to a processing unit (FPGA). In the FPGA the signal is sent through a *de-glitcher* that cleans up erroneous video lines, for instance due to switching. After the de-glitcher the video is sent to the *Audio de-embedders*, where audio is split from the video.

3.1.1 Audio data path

The stereo audio channels from the de-embedder are sent to an audio store buffer. The audio is fetched from the audio store buffer after the user specified delay. It is then sent to the *Audio matrix*.

Two other sources are available in the audio matrix: A 1 kHz stereo sine tone and a generated *muted sound* which is a legal audio stream with muted audio.

Outputs with missing inputs are routed to a fallback signal. The fallback signal may be silence or the tone generator.

Each output from the matrix is sent to an *Audio Processing Block* where channels can be processed or rearranged within the channel pair.

Finally, eight stereo pairs are routed to the *Audio Embedder* and the two remaining pairs are sent to the audio DAC and the AES output.

3.1.2 Video data path

The video is routed to an *aspect ratio converter block* and the resulting SD video is passed to a *Frame synchronizer block*.

An internal video generator can be switched in as a fallback source if the input video is missing.

The audio is re-embedded and the video then passes through a *Video processing block* with an integrated *Legalizer*, before entering an *EDH processing block*. Embedding of the EDH packet is configurable.

The parallel video is sent out of the FPGA and into a serializer that re-clocks the data and sends the SDI to a buffered output switch.

The output switch is used to bypass the video processing core so that DVB-ASI may pass through the module. The switch selects between the equalized and re-clocked input (*Through mode*) and the output from the FPGA(*Processed mode*).

The outputs of the first two switches are sent to two digital outputs and the third switch controls the signal sent to the video DAC.

3.2 Video blocks overview

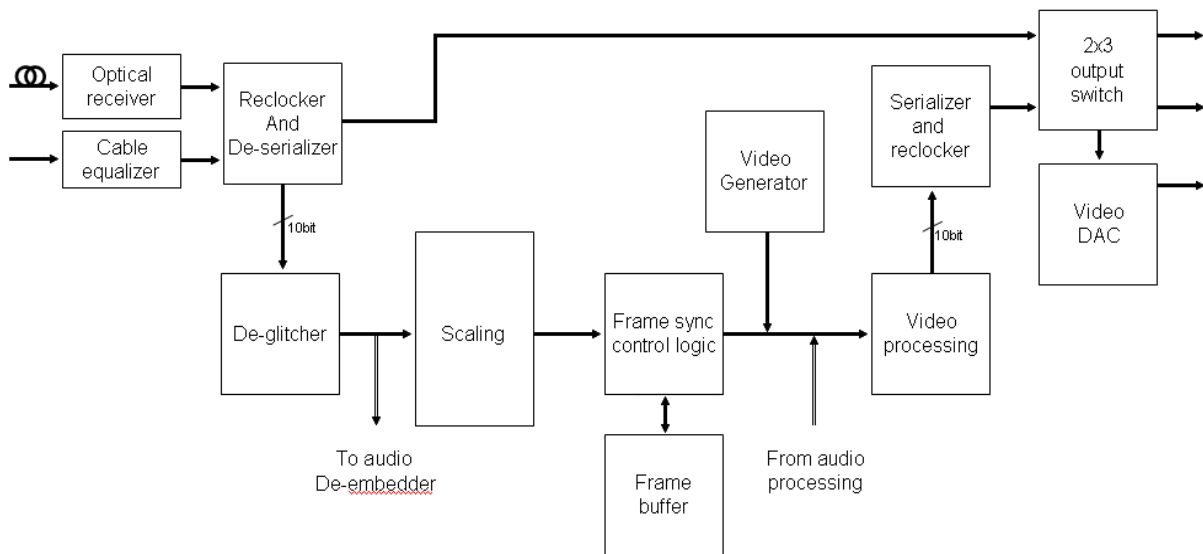


Figure 2: Video block diagram

3.3 Optical/ Electrical input selection

The ARC-SD-DMUX-R has both an optical and an electrical input. The active input can be either:-

1. Automatic selection based on a prioritized list of inputs and a selected rule of switching.
2. Manual selection.

When controlled by DIP switches, the card will use the fall back source and generator settings saved from the last Multicon GYDA session.

3.3.1 Automatic selection mode

Video in Mode set to *auto*: There are three priority levels. Each level may be assigned an input setting; optical, electrical, video generator or mute.

The priority is the order in which the board will look for a valid input. The card will switch to the next priority after a loss of lock of the input signal.

The module will not switch automatically back to a higher priority if the active source is the electrical or optical input. *Latch reset* will reset the active input to the main (highest priority) input.

Hold time determines how long a signal has to be missing/out of lock before it is considered lost. This is useful to avoid switching when the input has intermittent faults.

Lock time determines how long a higher prioritized signal has to be locked before it again can be considered to be present and stable. This is only active when the module has lost both optical and electrical video inputs.

3.3.1.1 If video input disappears

Given that stable SDI input and sync input exist: If the SDI input disappears and *Video in* is set to *Auto*, the board will hold on to the current input for the time set by *Hold time* whilst frame freezing.

The board will then select the next input in the priority list.

3.3.2 Manual selection mode

If the SDI signal disappears the board will frame freeze indefinitely.

3.4 De-glitcher

The de-glitcher corrects timing errors within a line of video due to source switching. This allows perfect synchronous switching.

Non-synchronous input switching will not produce any other artifacts than a freeze frame *if* the frame store has more than a full frame in the memory.

3.5 Aspect Ratio Converter block

The aspect ratio converter block is a 13 tap high quality linear resampling scaling engine. It may be used to stretch or shrink a picture vertically and horizontally. The picture may also be offset with respect to the centre of the picture.

The block can detect a change in aspect ratio information embedded in the input signal. The scaling will then be changed during the vertical blanking period allowing on-air automatic switching of aspect ratio conversion.

Externally triggered changes of aspect ratio are also deferred until the next vertical interval to allow the use of the module in a transmission signal path.

The module is intended to be used primarily to convert SD video between standard aspect 4:3 and widescreen 16:9.

The primary difficulty with the conversion is number of possible conversions. This can be greatly reduced by setting the output aspect ratio to be 4:3 or 16:9. We call this the **output environment**. The actual scaling will depend on the input signal.

The **output environment** setting actually describes the aspect ratio of the pixels. The **fill factor** is the term for the amount that the picture fills the output frame, the presence of horizontal or vertical curtains or black bars.

The output signal will have the appropriate AFD, VI WSS and S352M embedded. All of these metadata types may also be disabled.

There are four operational modes for the module:

1. AFD -> Frame fill setting -> default conversion
2. AFD -> default conversion
3. Frame fill setting -> default conversion
4. Fixed default conversion

The primary assumption for the first three modes is that an input signal with the same aspect ratio as the output environment *will not be scaled*. (There are a couple of exceptions if the picture has both horizontal and vertical curtains.)

In mode 4 the setting of the default scaling will be used for all input signals.

3.5.1 Automatic scaling modes

The following applies to the first three automatic modes of operation.

The scaling performed by the module is determined by the input picture aspect ratio and fill factor (presence of 'curtains') but normal SD video does not natively state what aspect the pixels are or if another conversion has already been applied. There are three sources of information that *may* be present in the video that can provide some or all of this information.

Active Format Descriptor (SMPTE S2016 referred to as AFD) and Video Index (SMPTE RP186 referred to as VI) describe both the aspect ratio and the fill factor of the picture.

However, the fill factor descriptor *may* contain a code to indicate that the fill factor of the picture is unknown. In that case, the code for the input aspect ratio is used.

SMPTE352M is a data packet that can be used to identify the aspect ratio of the picture.

Wide Screen Signaling present in the input video (WSS) can also be used to identify the aspect ratio of the picture but is not implemented yet (contact Nevision sales if this is a requirement).

3.5.1.1 Mode 1: Full automatic mode

The aspect ratio control block will start by looking for AFD presence in the input signal to select the aspect conversion. If it is not present it will look for VI and then SMPTE S352M information. If no aspect ratio information is present in the video, the default scaling setting will be used.

When a valid format descriptor is present, either from AFD or VI, all the conversions in the AFD code drawing are possible for the given output environment.

In the case where only input environment information is available, a subset of the conversions is used. The desired filling method must be set. This may be one of the following:-

- Full frame. The image will be zoomed and cropped. No curtains.
- 14:9 pillar box / letterbox. The image will be zoomed and cropped. Narrow curtains.
- 4:3 letterbox / 16:9 pillar box. The image will be zoomed. Full curtains.

If the input environment is the same as the output environment, no conversion will be performed.

3.5.1.2 Mode 2: AFD or default

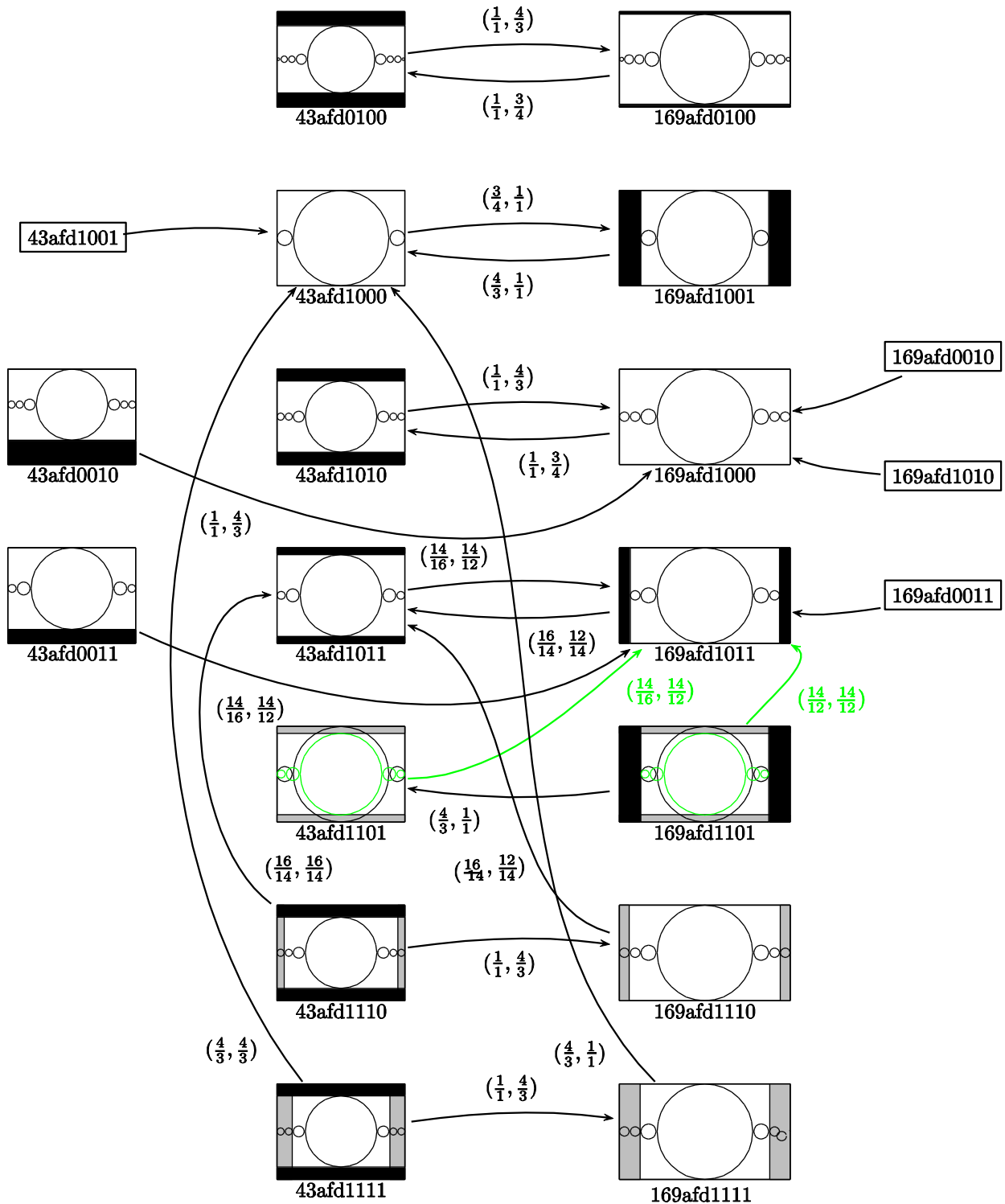
This mode will only use the AFD information if present. The default scaling will be used if there is no AFD packet, no video index or the active format descriptor is set to 'Unknown'.

3.5.1.3 Mode 3: Fill mode or default

This mode will only use the input aspect information from the AFD information if present. The S352M packet will be used if it is present and neither AFD packets nor VI are present. The default scaling will be used if there is no AFD packet, no video index and no S352M packet.

3.5.1.4 AFD conversions

The figure below shows the different transitions that are defined. The incoming format is given by the VI/AFD, and the user has supplied wanted output environment. Transitions from a state to itself are not shown to avoid clutter in the figure. The corresponding AFD format is shown for reference.



The figure looks confusing at first but observe that all the states have only one arrow leading from each state to the other column. This arrow defines the normal conversion when the input environment is different to the output environment. Find the picture type that you have on the input and follow the arrow which points out of that state to find the conversion that will be performed by the ARC-SD-MUX when the AFD code is present.

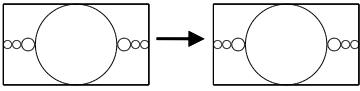
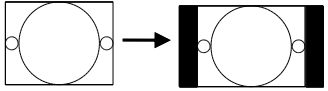
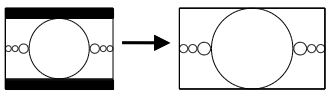
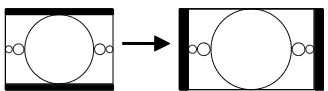
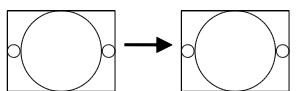
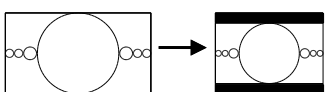
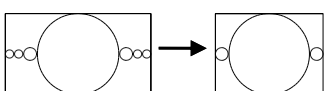
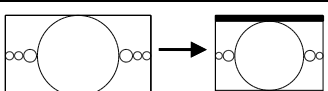
There are a few states where the input picture has both horizontal and vertical curtains and these also have arrows within the same column. These are conversions that will be performed when the input environment is the same as the output environment.

3.5.1.5 Fill mode conversions

If the module can not find any fill factor information but has aspect ratio information, it will perform one of three conversions when the input environment is different to the output environment.

1. Protect input frame.
2. Zoom to fill frame.
3. Zoom to 14:9.

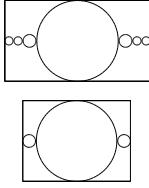
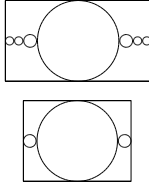
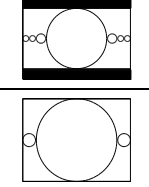
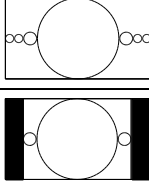
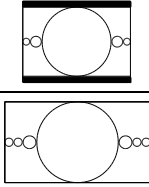
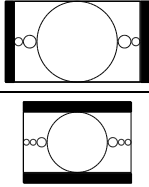
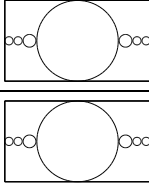
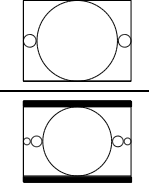
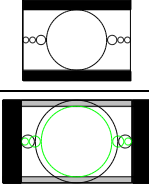
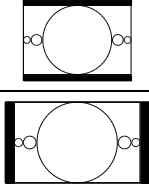
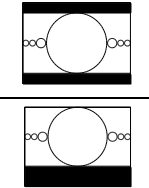
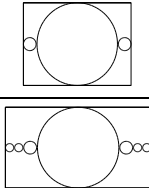

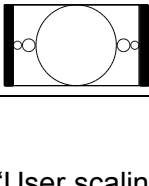
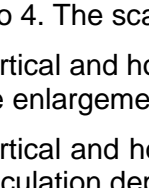
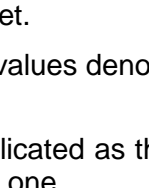
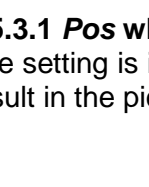
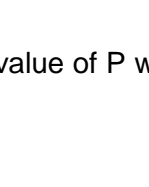

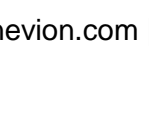
The table shows the conversions that will be performed when this mode is active.

Output Environment	Non-AFD Conversion	Input environment	Conversion performed
16:9	Any.	16:9	
16:9	Protect input frame	4:3	
16:9	Zoom to fill frame	4:3	
16:9	14:9	4:3	
4:3	Any.	4:3	
4:3	Protect input frame	16:9	
4:3	Zoom to fill frame	16:9	
4:3	14:9	16:9	

3.5.1.6 Default scaling mode

This mode is used when no information about the input video is detected by the ARC-SD-DMUX. This mode uses the fixed scaling setting. The scaling and offset of the output picture is fixed.

3.5.2 Pre-defined settings

Input	Conversion	Output
	No conversion	
	4:3 cropped to 16:9 full frame	
	4:3 to 16:9 with 4:3 pillar box	
	4:3 cropped to 16:9 with 14:9 pillar box	
	16:9 to 4:3 with 16:9 letterbox	
	16:9 cropped to 4:3 full frame	
	16:9 cropped to 4:3 with 14:9 letterbox	
	4:3 with 16:9 letterbox cropped to 4:3 with 14:9 letterbox (zoom 1.143)	
	16:9 with 4:3 pillarbox cropped to 16:9 with 14:9 pillarbox (zoom 1.167)	
	4:3 with 16:9 letterbox cropped to 4:3 full frame (zoom 1.333)	
	Top 4:3 cropped to 16:9 full frame	
	Top 4:3 cropped to 16:9 with 14:9 pillarbox	

3.5.3 User defined settings

It is possible to set the scaling values and AFD codes of four settings named "User scaling" 1 to 4. The scaling values control horizontal and vertical, zoom and centre offset.

Vertical and horizontal zoom can be adjusted within the range 0.5 to 1.5. The values denote the enlargement of the output image.

Vertical and horizontal centre offset or position values are slightly more complicated as the calculation depends on whether the active scaling zoom is greater of less than one.

3.5.3.1 Pos when zoom is less than 1:

The setting is in lines (vertical offset) and pixels (horizontal offset). A position value of P will result in the picture moving P pixels or lines.

3.5.3.2 Pos when zoom is greater than 1:

The setting is in lines (vertical offset) and pixels (horizontal offset) but the values are also scaled by the zoom factor. A zoom value larger than 1 with a position value of P will result in the picture moving (P x zoom) pixels or lines.

Positive position values moves image right/up, negative values left/down.

The embedded AFD code for each User setting may be set. Use the figure in the AFD conversion section to find the appropriate code.

3.6 Frame synchronizer

The frame synchronizer consists of a frame store buffer and some control logic. The frame store buffer can store up to 8 SD frames. The frame synchronizer is placed after the ARC block. The control logic sets the frame synchronizer either frame sync mode or frame delay mode of operation depending on the presence of the sync input signal.

If the sync input presence changes, the operational mode of the modules changes, resulting in frame roll.

3.6.1 Frame Sync mode

If a sync input (B&B or Tri-level) is present, the module will output a signal that has a constant relative timing to this signal. Two parameters can be set; output phase and minimum delay.

The output phase can be positive or negative and sets the timing offset between the sync input and the video output.

The minimum delay sets the minimum delay between video output and video input. The actual delay can be larger than the minimum delay (hence the name), because the card must also adjust the picture phase relative to the sync input.

The user may set the 'minimum delay' up to 7 frames.

3.6.2 Frame delay mode

This mode is active when a sync signal is not present. The minimum delay setting is then used directly. 1 frame and 1 line minimum delay means that the output will be 1 frame and 1 line delayed version of the input.

3.7 Video generator

The video generator can produce one of the signals from the following list:-

- Color bar
- Checkfield
- Color bar with moving black box
- Black
- White
- Yellow
- Cyan
- Green
- Magenta
- Red
- Blue

The flat field option allows the user to specify any combination of luma and chroma values.

In normal operation (as a fallback generator), the video generator will take its video standard setting from the last video input seen by the board.

To enable the board to act as a standalone and user configurable video generator, the video generator must be either set as the first priority input when *Mode* is *auto*, or selected manually by setting *Mode* to *Video generator*. This will override any video input but the generator signal will still be locked to the sync or SDI inputs, if present. For true standalone generator operation, the inputs should be removed. Available video standards are 486/25i and 576/25i.

3.8 Label generator

The label generator consist of 2 lines of 16 characters each that are placed at the lower left corner of the active video area.

The main function is to add a label to the internal generator on loss of input signal. The label may also be configured to be permanently present.

Note that to see the label on an output the video output selection must be set to “processed” for this specific output.

3.9 Video processing block

The video processing block consists of gain and offset adjustments and a video legalizer.

3.9.1 Gain and offset

The gain and offset adjustment is set separately on the Y, Cb and Cr samples.

	Range Multicon GYDA
Luma gain	0 – 3.999
Chroma gain	0 – 3.999
Luma offset (gain =1)	-511.75 – 511.75
Chroma offset (gain = 1)	-255.75 – 255.75

3.9.2 Video payload legalizer

The legalizer limits the upper and lower values of the video payload to the following values.

Upper limit	Luma:	3ACh
	Chroma:	3C0h
Lower limit	Luma:	040h
	Chroma:	040h

Even with the legalizer disabled, the video processing block limits luma and chroma to 3FBh and 004h respectively.

3.10 EDH processing block

If enabled, the EDH processing block extracts the EDH packet from the video, updates the EDH flags according to SMPTE RP165 and inserts the EDH packet into the ancillary data of the video.

If disabled, The EDH processing block only reads and reports the incoming EDH packet status and deletes the packet from the video stream.

3.11 Video output selection

The board has two non-inverting digital outputs and a group of three analog outputs. Each of the outputs and the analog group can take their respective signals directly from the input or from the output of the processing unit.

3.12 Video DAC

The video DAC has three outputs, with the following combinations available:

- CVBS/CVBS/CVBS
- CVBS/Y/C
- Y/Pb/Pr
- R/G/B

The board can handle 50Hz-based and 60Hz-based input signals but can not convert between them. The modulation setting is split in two; one to select between NTSC and PAL M output for 60Hz-based sources, and one to select between PAL B/G and PAL N for 50Hz-based sources.

The following modulations are available for CVBS and S-Video:

- PAL B/G
- PAL N
- NTSC
- PAL M

It is also possible to turn black setup (“pedestal”) on or off for NTSC.

3.13 Audio overview

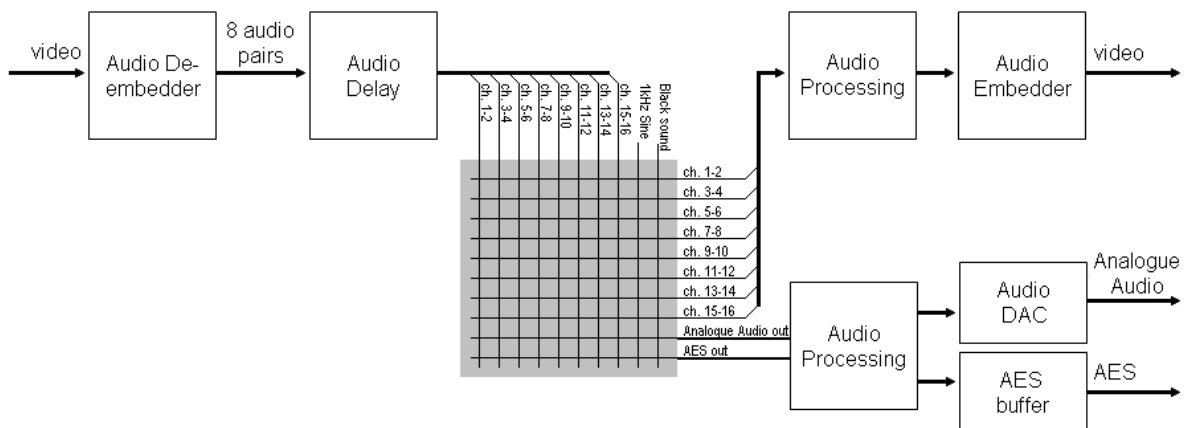


Figure 3: Audio function block

3.13.1 Audio de-embedder

The Audio de-embedder extracts all audio embedded in the video stream. The de-embedder is always enabled.

3.13.2 Audio delay

An audio delay can be specified relative to the video output. It is situated before the audio cross point matrix and is common for all de-embedded channels. The audio delay is specified in terms of 48 kHz audio samples and can be set to positive or negative values.

Note: As the audio delay is relative to the video output it is possible to specify an audio delay that will actually be too small. This will cause audio errors.

3.13.3 Audio cross point matrix

The audio cross point matrix is a 10x10 cross point with inputs and outputs as shown in Figure 3. The 8 de-embedded channels, a 1 kHz sine and “mute” are selectable inputs. “mute” is explained in chapter 3.1. The outputs of the cross points are 8 stereo channels for re-embedding, one analog audio output and one AES output.

3.13.4 Audio fallback options

The 10 output channels from the cross point matrix have configurable fallbacks, used when their corresponding sources are missing. The eight embedder channels have one fallback setting and the audio DAC channel and AES out have their own settings.

The priorities can be selected between *matrix* (being the selected channel in the cross point matrix) or the internally generated *sine*, *mute* or *delete/output off*.

3.13.5 Audio generator

The stereo audio generator is available as an input to the audio cross point matrix and as a fallback option. There are three slightly different ways to select the generator:-

- select it in the matrix directly
- select it as the first priority in the audio fallback setting
- select it as second priority behind a missing input

The generator signal is a high purity 1 kHz sine wave with a 250ms interruption on the left channel every 3 seconds. The audio level may be set to one of two standards, -18 dBFS and -20 dBFS. These two levels correspond to EBU R68 and SMPTE RP155.

3.13.6 Audio processing block

The output of each stereo signal from the audio cross point matrix has an audio processing block. This is controlled with the Multicon GYDA controller. The processing includes channel L/R manipulation and audio gain.

3.13.6.1 Channel L/R manipulation

The stereo signals may be output in one of the following ways:

- LR, Left / Right	No change.
- RL, Right/ Left	Channels are swapped.
- LL, Left/ Left	Left channel is copied into the right channel.
- RR, Right/ Right	Right channel is copied into the left channel.
- !LR, ØLeft/ Right	The left channel is phase inverted.
- !R, Left/ ØRight	The right channel is phase inverted.
- MM, (Left + Right)/2	The left and right channels are summed.
- MS, MS/AB	The left and right channels are converted from AB stereo to MS stereo.

The sum products (L+R/2 and MS) are reduced in level by 6 dB to avoid any possibility of clipping.

3.13.6.2 Audio gain

The gain may be set to +-96dB with a gain step of 0.1dB.

Note that non-audio data is ignored and left unchanged by the gain function.

3.13.7 Audio embedder

The audio embedder can be enabled and disabled per group.

A 24-bit audio signal uses the Extended Audio Data Packet for the 4 least significant bits. Not all equipment can handle Extended Audio Data Packets correctly, so the option exists to truncate all audio data to 20 bits. **This setting is common for all embedder channels.**

The insertion of Audio Control Packages can also be switched on and off. **This setting is also common for all embedder channels.**

3.13.8 Analog audio output

The maximum (clipping) level of the analog audio output can be adjusted in MULTICON GYDA. The resolution is 0.5dB (input will be rounded to nearest 0.5dB) and the range is from -95.5dBu to 24dBu. It is also possible to mute the output completely.

4 Configuration

4.1 DIP switch functions

The two sets of DIP switches are labeled with a number running from 1 to 15. The 16th DIP is labeled *OVR*. Note that the left DIP switch of the horizontal DIP package is number 1. The top DIP switch of the vertical DIP package is number 9. Default settings as delivered from factory should be all DIPs in the Off position. The module will then be under Multicon GYDA control, see description for DIP switch 16 below.

Table 1: DIP SWITCH FUNCTIONS

Switch #	Function name	Function DIPs	Comment
1	SDI OUT 2	Off: processed mode On: through mode	In through mode the video goes through a re-clocker only. For monitoring only, no aspect ratio conversion or other processing is performed.
2	Video DAC out	Off: processed mode On: through mode	In through mode the video goes through a re-clocker only. For monitoring only, no aspect ratio conversion or other processing is performed.
3 - 5	Aspect ratio conversion rule	[3 4 5]=[Off Off Off] => 4:3 -> 4:3 [3 4 5]=[Off Off On] => 16:9=>4:3LB [3 4 5]=[Off On Off] => 16:9 ->4:3FF [3 4 5]=[Off On On] => 16:9=>4:3 (14:9) [3 4 5]=[On Off Off] => 16:9 ->16:9 [3 4 5]=[On Off On] => 4:3 ->16:9FF [3 4 5]=[On On Off] => 4:3=>16:9PB [3 4 5]=[On On On] => 4:3=>16:9 w/14:9 PB	These 3 DIPs choose which parts of the picture are preserved or cropped away when aspect ratio must be performed.
6 - 7	SD video DAC format	DIP[6 7] = [Off Off] => CVBS DIP[6 7] = [Off On] => YPbPr DIP[6 7] = [On Off] => SVideo DIP[6 7] = [On On] => RGB	These two DIPs choose video DAC output format.
8	SD video DAC modulation	Off: PAL B/G + NTSC On: PAL N + PAL M	Selection between PAL B/G and NTSC or PAL M and PAL N is automatic, based on video input.
9	Black setup disable	Off: Black setup for NTSC On: No black setup	For NTSC only.
10	Input priority	Off: Optical input has priority On: Electrical input has priority	This switch has no effect for boards without the optical input (-R option).
11 - 12	Audio DAC and AES group	DIP[11 12] = [Off Off] => Gr1 DIP[11 12] = [Off On] => Gr2 DIP[11 12] = [On Off] => Gr3 DIP[11 12] = [On On] => Gr4	The 2 first of these 4 DIPS select one of the de-embedded groups.

Switch #	Function name	Function DIPs	Comment
13	AES + ADAC channel	Off: Ch1 On: Ch2 (from selected group)	This switch selects the audio channel pair within the selected group.
14	AES/Data link	Off: AES3 out on AES output On: Data link out on AES output	The two slide switches on the bottom side of the board must also be switched. See ch. 4.2.2 below.
15	RESET	Off: Use values preset by MULTICON GYDA On: RESET to factory defaults	This DIP is only read during boot. The board will not start when DIP 16 and this DIP are both set to On. After returning the DIP to normal position, the card must be restarted and kept powered for a minimum of 10s to complete the reset. The reset will only affect settings not pertaining to DIPs and the rotary switch.
16	OVR	Off: MULTICON GYDA mode On: Manual mode	This DIP is only read at power up. OVR is short term for MULTICON GYDA override.

4.2 FACTORY reset function

A factory reset is a 3 step process:

1. Set DIP 15 and DIP 16 to 'on' and boot the card.
2. Remove power and set DIP 15 to 'off'.
3. Power up card once again. The operation of the card will immediately reflect the freshly loaded default settings. However, the card must be kept powered for at least 10 seconds to ensure that these settings are stored locally to be retrieved again at the next start-up. The card's operational environment must also be kept static during those 10 seconds (i.e. no change in incoming video standard, no commands issued). Failing to meet this requirement could result in an incomplete reset and require the user to restart the factory reset sequence.

4.2.1 Rotary switch and push buttons

These functions are available.

The *rotary switch*, labeled DLY, adjusts the phase delay from -5 to +4 video lines. It is only functional when a sync signal is present at the sync input. The rotary switch is accessible from the board front.

The *push buttons*, labeled INC and DEC, are used to fine adjust the phase delay by samples. It can adjust $\pm 1/2$ video line. Pressing a button and keeping it pressed will accelerate the change. The LED adjacent to the button will flash for a short period of time when the end of the adjustment range has been reached. Pressing both buttons at the same time will return to the middle of the adjustment range and the board will acknowledge by flashing the INPUT and SYNC LEDs simultaneously.

4.2.2 Slide switches

The two switches at the top of the module (rear side) switch between AES out and Data out. The output signal is DC coupled when in DATA out mode and AC coupled when in AES mode.

Note that to enable Data link output on the AES connector it is also necessary to set DIP 8 to the Off position when the board is in Manual mode (DIP 16 = On), or when the board is in Multicon GYDA mode (DIP 16 = Off), to select Data link over AES output in Multicon GYDA. AES mode is with the slide switches moved to the right (as shown).

The switch on the left card edge switches between backplane sync input and Flashlink distributed sync (Future feature upgrade of Flashlink frame). Switch moved up routes the backplane sync to the card.

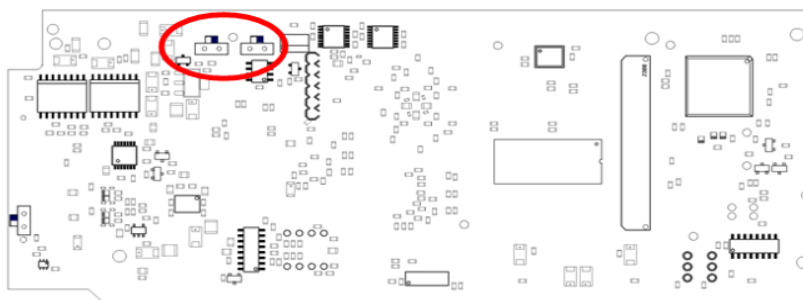


Figure 4: The figure shows a bottom view component printout of the board. Note the location of the slide-switches.

4.3 MULTICON GYDA mode

All functions of the card can be controlled through the MULTICON GYDA control system. The MULTICON GYDA interface has an information page and a configuration page.

4.3.1 Information page

The information page shows a dynamic block-diagram of the board and some additional information text. The block diagram self updates with the board status, showing selected input signal, missing signals (by red crosses over the appropriate signal lines) and signal routing (by graphic switches). It also shows the audio matrix selections that have been made in the configuration page.

Note that if a stereo pair of embedded audio is missing, the user will still be allowed to select that pair from the audio matrix. The output will however go to the fallback position immediately. A missing stereo pair will be shown in the block-diagram as a red cross over the appropriate matrix input line.

The video delay reflects the actual delay between input and output video.

The audio de-embedders 1-4 show the state of the audio control package for their associated audio group de-embedded from the input stream.

The audio embedders 1-4 show the state of the audio control package and the audio bit depth for their associated audio group embedded in the output stream.

Embedded UART shows the data rate of the data link embedded in the audio control packages on the incoming signal.

4.3.2 Configuration page

The different configuration possibilities are explained in Chapter 3, under the corresponding blocks or functions.

5 Connections

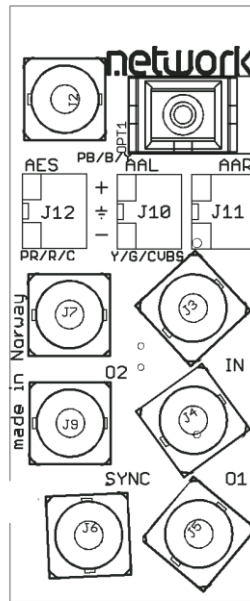


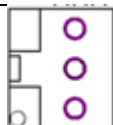


Figure 5: ARC-SD-DMUX-R backplane

The backplane for the ARC-SD-DMUX is called DWC-HD-DMUX-C1. The table below shows the connectors and their functions.

Function	Label	Connector type
SD-SDI input	IN	BNC
SD-SDI output 1	O1	BNC
SD-SDI output 2	O2	BNC
Analog video, Y/G/CVBS	Y/G/CVBS	BNC
Analog video, Pb/B/Y	PB/B/Y	BNC
Analog video, Pr/R/C	PR/R/C	BNC
Sync input	SYNC	BNC
Analog audio out left channel	AAL	WECO Audio connector
		
Analog audio out right channel	AAR	WECO Audio connector
		
AES out	AES	WECO Audio connector
		
Optical input	OPT1	BSC-II (for SC input)

6 Operation

6.1 Front panel LED indicators

Diode's state	Red LED	Orange LED	Green LED	No light
Card status	PTC fuse has been triggered or FPGA loading has failed	FPGA loading. If constantly lit for more than a few seconds: DIPS 15+16 both set to the 'On' position, or module not programmed	Module is OK	Module has no power
SDI input status	Video signal absent	Video signal present but card not able to lock VCXO	Video input signal in lock	Module not programmed, or DIPS 15+16 both set to the 'On' position
Sync input status	Sync signal absent	Sync signal present but card unable to lock VCXO	B&B or Tri-level sync in lock	Module not programmed, or DIPS 15+16 both set to the 'On' position
Audio input status	No audio embedded in incoming video	One, two or three audio groups embedded in incoming video	4 audio groups embedded in incoming video	Module not programmed, or DIPS 15+16 both set to the 'On' position

Note that three special conditions also exist: When all four LEDs blink synchronously, this is the result of the '*locate on*' command. This condition will eventually time out but can also be reverted by issuing the '*locate off*' command.

The second special condition is when an FPGA firmware upgrade is performed: When Multicon GYDA is finished transferring the compressed data file, the card will spend some time unpacking this file and during this time it will not respond to commands or update settings. During this time it will display running lights (three LEDs lit, one dark, the position of the dark LED will move around).

The last special condition is when the user adjusts the phase delay with the push buttons at the front of the card. Short flashes on the SYNC or INPUT LEDs means that the end of the adjustment range has been reached. If they flash simultaneously, both push buttons have been pressed simultaneously and the samples part of the phase delay reset to the middle of the adjustment range.

6.2 RS422 commands

6.2.1 FLP4.0 required commands

Block	Blk #	Commands	Example	Response	Control
-	-	?	?	product name\ SW rev n.m\ FW rev r.s\ protocol ver 4.0\ 	Hello command. <i>Note 1: No other commands will be available until the card has received this hello.</i> <i>Note 2: This command will also enable checksums.</i> <i>Note 3: Cards are designed to be hot-swappable. To sync with the start of a new command, the cards will wait for a <lf> character before looking for a valid command.</i>
conf	0	-	conf 0	*too long to list*	Configuration settings Retrieves the card's configurable settings. Each addressable block is represented by a single line. Dynamic status <i>may</i> be included in response, but is usually reported in <i>info</i> only.
-	-	info	info	*too long to list*	Dynamic status info Blocks with static settings only will usually not be included, see <i>conf</i> above.
-	-	chk off	chk off	ok	Checksum off If issued twice in succession, this command will disable checksums. Note: Responses will still have the checksums appended. <i>NOTE1: ? command turns the checksum on again</i>
-	-	locate on <seconds> locate off	locate on 3 locate off	ok	Card locator This command will cause all the LEDs to flash for a user specified number of seconds. If omitted, the value <seconds> will be set to a default of 120 seconds. The flashing can be terminated at any time with <i>locate off</i> .
-	-	address	address	address <address>	Card address This command will force the module to check and update its current rack and slot address. This is normally only done at start-up.
-	-	filename	filename arcsddmux-0-101.ffw	<name>'.<extension>	Firmware update The <name> part must match the card's hardware and include a revision number, and the extension must be either 'ffw' for FPGA firmware or 'mfw' for microcontroller firmware. After running this command the board will be ready to receive its new firmware in Intel-hex format.
-	-	fin	Fin	ok	Finalize Finalize the programming of the microcontroller. See description of the uC boot loader (separate document).

Block	Blk #	Commands	Example	Response	Control
misc	0	-	STATUS NOT AVAILABLE BY COMMAND, ONLY FOUND in <i>conf 0</i> AND <i>info</i> RESPONSES!	prog fin '' ovr	<p>Misc info</p> <p><i>prog</i> if the card is freshly programmed by the boot loader and the program is still un-finalized. <i>fin</i> is the normal condition.</p> <p><i>ovr</i> if DIP-switch 16 is set to the ON position and the card is under DIP-switch control.</p> <p>Note 1: The info part of misc has additional functionality when locate is used: <i>locating <remaining seconds></i>. This enables a visible countdown clock in Multicon GYDA, but is not a required part of FLP400.</p>

6.2.2 Normal control blocks

Block	Blk #	Commands	Example	Response	Control
pin	0	on off	pin 0 on pin 0 off	cd ncd	Pin diode for optical input. No control available, except to turn power to the pin diode on or off. The info string reports <i>carrier detected</i> or <i>no carrier detected</i> .
ceq	0	-	ceq 0	cd ncd	Cable equalizer for electrical input. No control; only used to report <i>carrier detected</i> or <i>no carrier detected</i> .
cho	0	pri <k> pri <k> <l> pri <k> <l> <m> pos man <k> pos auto latch reset t1 <hold_time> t2 <lock_time>	cho 0 pri 0 cho 0 pri 0 1 cho 0 pri 10 2 cho 0 pos man 1 cho 0 pos auto cho 0 latch reset cho 0 t1 1000 cho 0 t2 1000	size 3 pri <i>k,l,m</i> auto t1 <hold time> t2 <lock time> size 3 pri <i>k,l,m</i> man m t1 <hold time> t2 <lock time>	<p>Video input select</p> <p><i>pri</i>: a prioritized list of inputs, used when change-over is automatic. The command can have 1, 2 or 3 entries, or <i>levels</i>. Manual mode is effectively the same as automatic mode with one priority level only, but has its own command.</p> <p>0 = from optical input 1 = from electrical input 2 = internal video generator 3 = mute 4 = none</p> <p>The card will always reply with 3 priorities, and converts any user input to 4=none for the priorities that are logically unreachable, i.e. a generator that is always present has a higher priority.</p> <p>.</p> <p>t1 and t2: change-over doesn't happen immediately, as a precaution against glitches and unstable signals. The timers t1 and t2 let the user decide how long (in ms) we will cling on to a missing input before we consider it gone and move on to the next pri level, and how long an input with a higher priority should be present before we consider it repaired and switch back, respectively.</p> <p><i>Note 1: the latch setting only applies to rule los.</i></p> <p><i>Note 2: the card change back to physical inputs from generators regardless of latch setting. As a side note, this means that t2 is important even when rule=lol and/or latch is on.</i></p> <p><i>Note 3: If we have selected rule=lol and a 3-level pri list with two physical inputs on top and a generator at the bottom and we're in generator mode (lost both physical inputs) and both physical inputs reappear at more or less the same time, which physical input will be chosen is unpredictable. This again due to having one reclocker only and having to hunt for</i></p>

Block	Blk #	Commands	Example	Response	Control
					<i>a valid input in the background while the generator is still selected.</i>
cho	1			size 3 pri <i>k,l</i> auto	Video fallback setting Second video change-over. This is generated from the settings in the first video change-over. No user settings.
cho	2-11	pri < <i>k</i> > pri < <i>k</i> > < <i>l</i> >	cho 2 pri 1 cho 5 pri 0 2	size 4 pri <i>k,l</i>	Audio fallback setting Audio change-over blocks, one cho per audio output from the audio matrix, mtz 0. No other settings but the priority list. 0 = from audio matrix 1 = sine 2 = mute (=silence) 3 = kill output (=no AES/ no embedding) <i>Note: Only generators (pri 1, 2 or 3) are allowed to be set as first and only priority.</i>
cho	12	pri < <i>k</i> > pri < <i>k</i> > < <i>l</i> >	cho 12 pri 1 cho 12 pri 0 2	size 4 pri <i>k,l</i>	Audio common fallback setting A short-cut to set change-overs 2-11 all at once. Will of course not report anything in info, that's left to the individual cho blocks.
cho	13	pos man < <i>k</i> >	cho 13 pos man 0 cho 13 pos man 1	size 2 man <i>k</i>	AES output select This change over has only manual mode and works as a simple 2:1 switch. 0: AES is selected 1: Embedded UART is selected
cho	14	pos man < <i>k</i> >	cho 14 pos man 0 cho 14 pos man 1	size 2 man <i>k</i>	EDH insert select This change over has only manual mode and works as a simple 2:1 switch. 0: EDH off 1: EDH on
cho	15	pos man < <i>k</i> >	cho 15 pos man 0 cho 15 pos man 1	size 2 man <i>k</i>	SDO 1 output select This change over has only manual mode and works as a simple 2:1 switch. 0: Through mode (re-clocked only) 1: Processed mode (from FPGA)
cho	16	pos man < <i>k</i> >	cho 16 pos man 0 cho 16 pos man 1	size 2 man <i>k</i>	SDO 2 output select This change over has only manual mode and works as a simple 2:1 switch. 0: Through mode (re-clocked only) 1: Processed mode (from FPGA)
cho	17	pos man < <i>k</i> >	cho 17 pos man 0 cho 17 pos man 1	size 2 man <i>k</i>	Video DAC output select By default set to processed mode
rcl	0	-	rcl 0	lock lol	Reclocker. No control; only used to report <i>lock status</i> .
emb	0-3	en dis acp (on off) use24 (on off)	emb 0 en emb 2 dis emb 1 acp on emb 3 acp off emb 1 use24 on emb 2 use24 off	(en dis) use24 (on off) acp (on off) del (off (on <del12> <del34>))	Audio embedder block en/dis: Enables or disables the embedding of the group into the ancillary area. acp on/off: This is valid only for SD

Block	Blk #	Commands	Example	Response	Control
		del (off (on <del12> <del34>))	emb 0 del off emb 2 del on 54 -432		and enables the audio control package. use24 on/off: This is only valid for SD and selects between 24bit and 20bit sound. del off/on delay12 delay34: For each of the embedder groups the delay bits for ch1+2 and for ch3+4 can be inserted into the ACP. The delay value can be positive and negative and is put directly into the ACP as it is written. <i>Note: To set both delays to 0 would be the same as turning the delays off. The response reflects this.</i>
demb	0-3	-	demb 0 demb 2	grp k en	Audio de-embedders one permanently assigned to each incoming group, always enabled. No control available.
scale	0-11	out env (16/9 4/3) out afd <afd-code>	scale 0 out asp 16/9 scale 0 out asp 4/3 scale 0 out afd 8 scale 0 out afd 11	out zoom <Hscale> <Vscale> pos <Hpos> <Vpos> env (16/9 4/3) afd <AFD-code>	Premade scale blocks. 12 fixed scale settings. The user can only change output environment and output afd-code.
scale	12-15	out zoom <Hzoom> <Vzoom> out pos <Hpos> <Vpos> out env (16/9 4/3) out afd <AFD-code>	scale 12 out zoom 1.33 1.33 scale 12 out pos 0.002 0.002 scale 12 out env 16/9 scale 12 out env 4/3 scale 12 out afd 8 scale 12 out afd 11	out zoom <Hscale> <Vscale> pos <Hpos> <Vpos> env (16/9 4/3) afd <AFD-code>	User scale blocks. Four user scale settings. Zoom: Zoom range is from 0.5 to 1.5. Position: Position when zoom is < 0 defines where in the output frame the box is placed. The box will never move outside of the frame. When zoom is > 0 the position defines which part of the input picture to use. A value of 0 is center. Positive values moves picture to the right or up. Negative values moves picture to the left or down.
scale	16	out env (16/9 4/3) out fill (full crop 14/9) rule <rule-value> ins <insert-value>	scale 16 out env 16/9 scale 16 out fill full rule 0x02 insert 0x20	scale 16 out env 16/9 fill full rule 0x1 use 0xF ins 0x20 use 0x3E	Master scale control block This block sets the conversion mode of the card and what aspect ratio information will be inserted in the output video. Output environment: out env can be 16/9 or 4/3. This controls the pixel aspect ratio of the output video. Fill: Fill selects how much of the picture is preserved. full: protect input frame crop: zoom to fill frame 14:9: scale to 14:9 PB or LB

Block	Blk #	Commands	Example	Response	Control
					<p>Rule: <rule-value> can take on the following values, and tells the card which incoming aspect ratio information to use: 0x01: AFD -> Fill -> Default 0x02: AFD -> Default 0x04: Fill -> Default 0x08: Default No other values will be accepted by the card, no combinations are available.</p> <p>Insert: The <insert -value> can be any binary combination of the following values: 0x02: WSS Extended 0x04: WSS 0x08: SMPTE352 0x10: Video Index 0x20: AFD Note that the value 0x01 is not currently supported, and that the card therefore will only accept even numbers as <insert-values>.</p>
vprc	0	lglz on lglz off (y cb cr) <gain> <offset>	vprc 0 lglz on vprc 0 lglz off vprc 0 y 1.03 4.0 vprc 0 cb 0.96 0.0 vprc 0 cr 1.34 -3.23	lglz (on off) y <ygain> <yoffset> cb <cbgain> <cboffset> cr <crgain> <croffset>	Video processing block Gain and offset must be given as floating point numbers. Gain is limited to [0, 4> for luma and chroma, while offsets are limited to <-1024, 1024> for luma and <-512, 512> for chroma.
sync	0	-	sync 0	lol (lock (rilvl bb sdi))	Sync block Frequency reference for video output. Status only, no commands available.
dly	0	<frames>frms <lines>lines <samples>sps	dly 0 2frms dly 0 2lines 30sps dly 0 0frms 50sps dly 0 0frms 3lines 50sps	tgt <frames> frms <lines> lines <samples> sps	Video delay This sets the minimum video delay of the card. In info this block reports back the current delay in nanoseconds. This will vary with the incoming video standard.
dly	1	<audio_samples>sps	dly 1 -30sps	tgt <audio_samples> sps	Audio delay The audio delay is given in audio samples. Audio delay is always given relative to video.
dly	2	<lines>lines <samples>sps	dly 2 1lines -30sps	phase <lines> lines <samples> sps	Video phase If lines != 0 the resulting phase will vary with incoming video standard, see dly 0 above.
vgen	0	cbar chkfield white yellow cyan green magenta red blue black mcbars	vgen 0 cbar vgen 0 flat 200 0 100 vgen 0 video 576/25i vgen 0 video 486/29i vgen 0 wss auto vgen 0 wss on 7	video <lns>/<rate><scan > wss (auto off (on <wss_value>)) (cbar chkfield white yellow cyan green magenta red blue black mcbars (flat <Y> <Cb> <Cr>))	Internal video generator. The video generator will be activated in two different ways: If selected as a fallback option the generator will generate the selected pattern when the other input(s) are missing, and then use the video settings from the last external source present. It can also be selected as the main input in cho 1, in which case its own video settings will also be used. cbar denotes colorbar, while mcbars

Block	Blk #	Commands	Example	Response	Control
		flat <Y> <Cb> <Cr> video <Ins>/<rate><scan> wss (off (on <wss_val>))			denotes colorbar with an superimposed moving black box.
vdac	0	cvbs ypbpr rgb svideo palbg palm paln ntsc bsetup (on off) wss (auto off (on <wss_val>))		vdac 0 fmt (cvbs ypbpr rgb svideo) mod (palbg paln) (ntsc palm) bsetup (on off) wss (auto (on off) on off)	Video DAC The module can handle 50Hz- and 60Hz-based sources, but can't convert video material between these time bases. The user must therefore select two modulations, one for 50Hz-based sources and one for 60Hz-based sources. The (on off) immediately following the wss auto is a status telling if the WSS bits are currently in use.
edh	0	msk <24b_mask> reset	edh 0 msk 0xFE00 edh 0 reset	msk <24b_mask>	Error detection and handling Error counting. The count itself is reported in info. Errors can be masked off and not counted; this is the purpose of the mask. The counter itself is 16b and will wrap around, but can also be reset by issuing <i>reset</i> .
mtx	0	<i1> <o1> ...<iN> <oN> <i1> <o1>,<o2>,...<oN> <i1> <o1> - <o2> ..or the above combined	mtx 0 0 2 1 4 5 5 mtx 0 0 0, 1 1, 2 2 mtx 0 0 0-9 mtx 0 0 0 1 1 2 2-9	size M:N i1 i2 i3... iN	Audio matrix mtx 0 (size 10:10) controls the audio matrix; outputs 0-7 are embedded sound, 8=adac and 9=AES. <i>Note: Any combination of the three basic commands are allowed, for instance the following command to set up a 10x10 audio matrix in a single line:</i> <i>mtx 3 1 1 2 2 3 0,3-9</i> <i>=> mtx 3 size 10:10 3 1 2 3 3 3 3 3 3</i>
mtx	1		mtx 1 10 0 mtx 1 1 0 mtx 1 0 0	mtx 1 size 16:1 10 mtx 1 size 16:1 1 mtx 1 size 16:1 0	Default scaler matrix mtx 1 (size 16:1) controls scaling to use when default scaling is selected.
mtx	2		mtx 2	mtx 1 size 16:1 10	Active scaling used mtx 21 (size 16:1) Tells which scaling is used.
agen	0	lvl <sine_level>cBFS	agen lvl -180 agen lvl -200	sine 1kHz lvl <sine_level>cBFS	Audio generator The amplitude of the generated sine that can be chosen as fallback in audio change-overs. Legal values are -180cBFS or -200cBFS (centiBel referred to full scale output). Units are optional, but if included must be written as cBFS (case sensitive).
aprc	0-9	lr rl ll rr nlr lnr mm ms	aprc 0 lr aprc 3 ll aprc 9 mm	lr rl ll rr nlr lnr mm ms	Audio processing one block for each output from cho 2-11. Outputs 8+9 are adac and AES, the lower 8 are routed to the embedder. The meaning of the commands are as follows: lr = Normal rl = Channel swapped ll = Left channel to both output

Block	Blk #	Commands	Example	Response	Control
					channels rr = Right channel to both output channels nlr = Left channel phase inverted lnr = Right channel phase inverted mm = Mono, both channels = (r+l)/2 ms = Mono/stereo, m=(l+r)/2, s=(l-r)/2
ablk	0	mute (on off) lvl <level>	ablk 0 mute on ablk 0 mute off ablk 0 lvl -500 ablk 0 lvl 30	dac lvl <level>cBu mute <mute_status>	Audio DAC control This word <i>dac</i> identifies this audio block as a DAC. The outputs can be muted, <mute_status> given as <i>on</i> or <i>off</i> , and the output level can be set in cBu (tenth dBu). Units are optional, if included must be written as <i>cBu</i> (case sensitive). Note 1: The lvl and mute are independent, so that the card will remember the lvl setting (and change lvl setting) while muted. Note 2: The resolution of the lvl control is 0.5dB but the card will perform correct rounding to nearest legal value and report the resulting setting. Legal input range is [-957cBu, 247cBu], representing the range [-95.5dBu, 24.5dBu].
supr	0	(en dis auto) font lb <label_page> <ASCII00> <ASCII01> ... <ASCII15>	supr 0 auto supr 0 font 0x4e4 supr 0 size 10 supr 0 lb 0 65 66 67 0	supr 0 font 0x4e4 lb 0 65 66 67 0	Video label The video label is a text string that is superimposed on the video. This feature can be enabled (en) at all times, disabled (dis) at all times, or enabled only when the internal video generator is active (auto). Maximum string length is 32 characters, over maximum 2 lines. The linefeed character (ASCII 10) is counted as one character, leaving 31. Strings can be terminated at any time using ASCII 0. There's an implicit ASCII 0 on the 33 rd character place. The example string on the left will display 'ABC' on a single line. The 32 characters are transmitted in two pages of 16 characters each. These pages are prefixed 'lb 0' and 'lb 1'.
uart	0	-		tx	The embedded data link, selectable by cho 13. No control possible, the word tx indicates that this is a transceiver only. Uart info reports link status: <i>los</i> (loss of signal), <i>raw</i> , or the speed of the embedded link (example: <i>115200/8/n/1</i>).

6.2.3 Commands intended for debug/lab use only

Block	Blk #	Commands	example	Response	Control
spir	-	<address>	spir 0x0004		Read a single word (or byte) from a SPI registers to check register status. Addressing is 16b and most significant nibble determines which chip. These are the address ranges: 0x0000 – 0x0fff : audio DAC 0x1000 – 0x1fff : FPGA 0x2000 – 0x2fff : flash 0x3000 – 0x3fff : deserializer 0x4000 – 0x4fff : serializer 0x5000 – 0x5fff : shift register (for LEDs) 0x6000 – 0x7fff : video DAC Note: The video DAC is actually using I2C, but the addresses are mapped into the SPI address range.
spiw	-	<address> <data>	spiw 0x0004 0x2c		With the same address ranges as for spir above, this command allows single SPI registers to be modified. Modifying SPI registers in the flash area is strongly discouraged!

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
 - Operating room temperature range: 0°C to 45°C
 - Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:
 - Temperature range: -10°C to 55°C
 - Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the “Administrative Measure on the Control of Pollution by Electronic Information Products”. In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

組成名稱 Part Name	Toxic or hazardous substances and elements					
	鉛 Lead (Pb)	汞 Mercury (Hg)	鎘 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
ARC-SD-DMUX ARC-SD-DMUX-r	○	○	○	○	○	○
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.						
X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.						

This is indicated by the product marking:



A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site <http://www.nevion.com/>. Please contact Nevion’s Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.