



ADC-AES8

Audio Converter Module

User manual

Rev. B

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Revision history

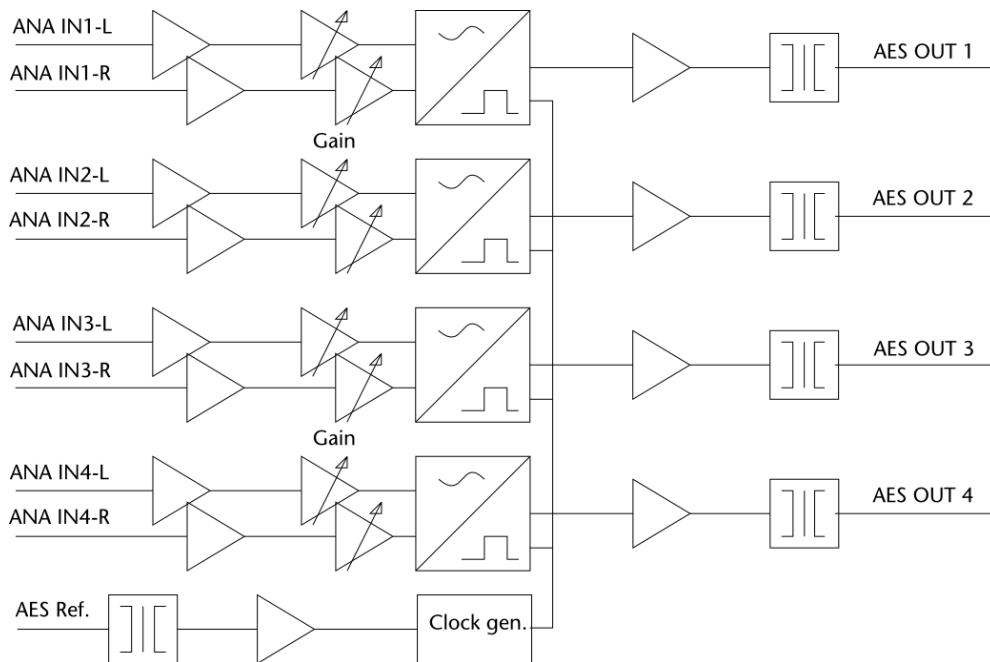
Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
B	1	2015-05-14	MB	Cover page; DoC removed; no other changes to content
1	-	2012-03-16	MDH	First Release

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1 Product overview



The ADC-AES8 has four stereo audio A/D converters on a single module. The module may be used as a normal Flashlink module in the original frame, N boxes and Flashcase. The module may also be used in the new frame in the half width slots as an auxiliary module for the Flashlink XMUX embedder modules.

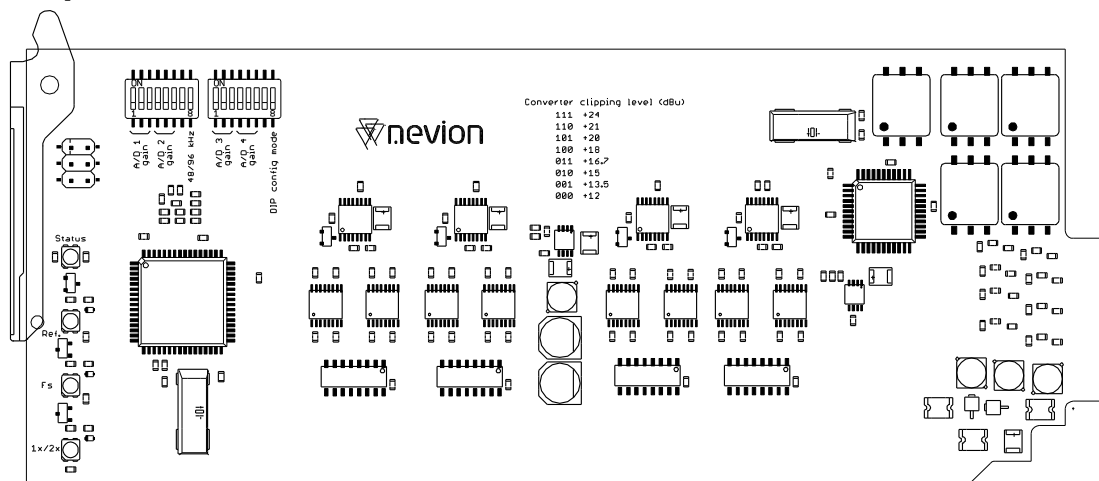
The gain of the converters may be set on the DIP switches on the module or with the GYDA Multicon system controller. The gain settings on the A/D converters are discrete levels.

The converters are calibrated with low impedance sources and high impedance terminations. The inputs are fully compatible with 600 ohm outputs. True 600 ohm inputs are available through special backplanes.

The A/D converters may be synchronized to an external AES3 signal with a sample frequency from 24 kHz to 96 kHz.

The A/D converters' internal clock may be configured to 48 kHz or 96 kHz. The module will use the sampling frequency present at the reference input, when present.

1.1 Top view



2 Specifications

2.1 A/D converters

Differential input impedance:	24 kohm
Common mode input impedance:	50 kohm
Maximum signal level (0 dBFS):	+12, +13.5, +15, +16.7, +18, +20, +21 or +24dBu
Level precision:	± 0.1 dB where $Z_{source} < 40$ ohm
Common mode voltage tolerance:	± 30 V – (Maximum peak signal level)
Frequency response:	20 Hz – 20 kHz ± 0.1 dB
Pass-band ripple:	± 0.005 dB
Stop band attenuation:	90 dB
Dynamic range ¹ :	Min. 103 dB (A) ² Typ. 105 dB (A) 0 dBFS = +18dBu
THD+N @ -1 dBFS:	Max. -85 dB, typical -90 dB
Intermodulation distortion ³ :	Max. -90 dB, typical -95 dB
Crosstalk:	Max. -90 dB, typical -99 dB
CMRR (20 Hz – 15 kHz):	Max. 80 dB @ 15 kHz, typical -85 dB @ low frequencies
Internal Sampling frequency:	48 or 96 kHz
Reference sample frequency:	from 24 to 96 kHz
Digital outputs:	AES3 110 ohm.

2.2 Power

+5V	0.200A	1.0W
+15V	0.050A	0.75W
-15V	0.047A	0.71W

¹ |THD+N of -60 dBFS 1 kHz signal| + 60.

² Dynamic range is a function of full scale level. Minimum result is obtained with 0dBFS = +12dBu

³ Signal at -12 dBFS, SMPTE 4:1 60 Hz + 7 kHz.

3 Configuration

The module has two main configurable parameters.

1. Converter gain
2. Internal clock frequency 48 or 96 kHz.

As all Flashlink modules, the module either uses the internally stored configuration, or uses the configuration on the DIP switches. The DIP switch labeled 'DIP config mode' controls this behavior.

3.1 DIP configuration mode

SW2.8 is the DIP config mode switch.

On: The card will be configured with the other DIP switches. The module will not accept commands from the system controller but may be monitored.

Off: The module will be configured with the internally stored configuration and may be controlled with FLP4 commands as listed in chapter 6.

As with all Flashlink modules, stored configurations in the Multicon controller will be applied to a module that is plugged into a running system, provided that the switch is off and that the last module present in the system was of the same type.

A module with SW2.8 on, plugged into a running system will overwrite the stored configuration in the Multicon controller with its own configuration.

3.1.1 Converter gain

The DIP switches are grouped as sets of three switches for each of the stereo converters. The levels correspond to the maximum sine wave level, otherwise known 0 dBFS.

Switches	000	001	010	011	100	101	110	111
Max. level (dBu)	+12	+13.5	+15	+16.7	18	+20	+21	+24

These values are chosen as being the most used levels in the broadcast industry. Custom values are available, contact Nevion support or your local sales representative. A/D Internal Clock frequency

3.1.2 A/D internal clock frequency

SW1.8 controls the A/D converter clock when there is no signal at the external reference input. If the switch is in the off position, the internal sample rate of the converters is 48 kHz. Otherwise, the internal sample rate of the converters is 96 kHz.

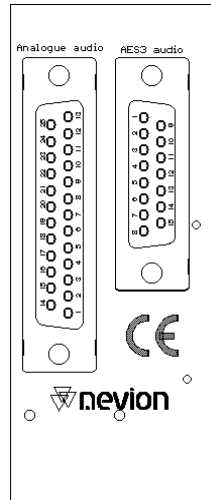
3.2 Multicon control

The module may be monitored and controlled with the Multicon system controller. The converter gains and A/D internal clock frequency may be remotely controlled through the module's configuration page of the system controller.

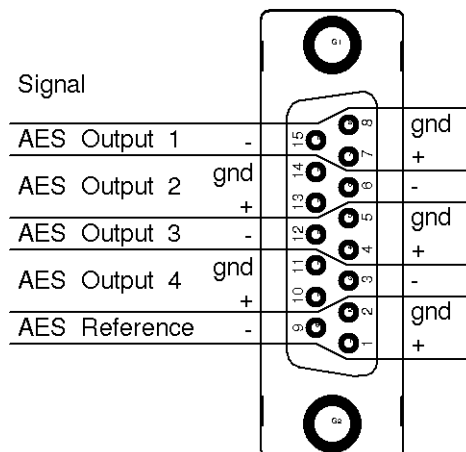
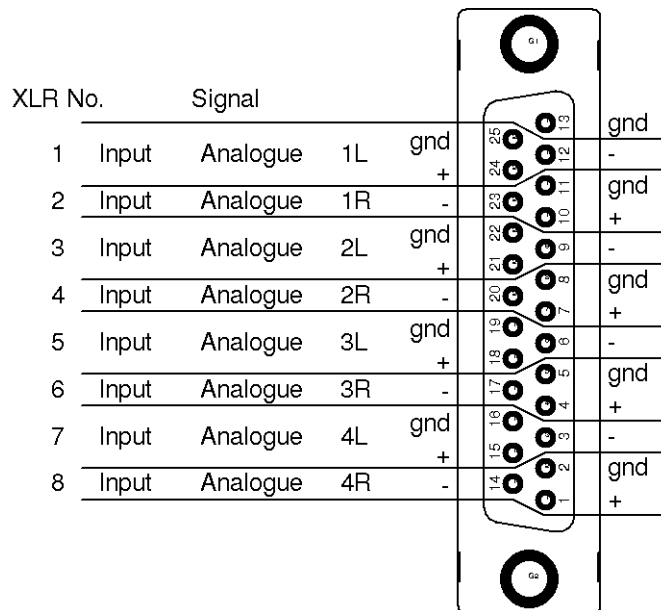
The AES digital audio input signal presence and the onboard power levels are presented on the info page. Alarms are generated for AES input loss (including the external reference) and power supply violations.

4 Connections

The standard backplane supplied with the ADC-AES8 is the ADDA-AES8-C1.



This backplane uses the standard pin assignment for the female DB-25 and a similar one for the female DA-15 as shown below.



5 Operation

5.1 LEDs

The module has four LEDs.

5.1.1 Status

The Status LED is green when the module is programmed and functioning normally. It will turn red for 1 second when power is applied and then turn green. Orange indicates that the module is not programmed, or is in the process of being programmed. It will turn red if there is something wrong with the power supply levels.

5.1.2 Sync

The sync LED is green when the external AES sync signal is received correctly.

The LED is red if there is no input or the signal has errors.

5.1.3 Fs and 1x/2x

The colours of the lower two LED shows the sampling frequency of the module is in the following table.

1 LED sample frequency display

Fs colour	1X/2X colour	Sample frequency
Green	Green	48 kHz
Orange	Green	44.1 kHz
Red	Green	Other Fs < 64 kHz
Green	Orange	96 kHz
Orange	Orange	88.2 kHz
Red	Orange	Other Fs > 64 kHz

6 FLP4 commands

FLP stands for Flashlink Protocol. The current revision of this protocol is 4, hence FLP4. This specification is available from Neviaon Support.

The following FLP4 block commands are used in the monitoring and control of the module.

- ablk
- pwr

6.1 ablk

The 'ablk' blocks correspond to the physical audio ports as follows.

Block no.	Audio Port
0	A/D stereo input 1
1	A/D stereo input 2
2	A/D stereo input 3
3	A/D stereo input 4
4	AES reference input

Blocks 0 to 3 report and accept the 'lvl' keyword followed by the maximum input level in cBu (dBu multiplied by 10).

i.e. ablk 0 lvl 240 cBu

Blocks 4 to 6 report input presence with the 'freq' keyword followed by the received sample frequency or 'los' or 'lol'. Absence of signal is reported with 'los' while 'lol' indicates an unrecognized sample frequency.

i.e. ablk 4 input freq 44 kHz

6.2 pwr

The 'pwr' blocks from 0 to 4 list the levels of the power supplies as measured by the microcontroller.

- 0 is the frame +5V
- 1 is analogue +4.8V
- 2 is the frame +15V
- 3 is the frame -15V
- 4 is digital +3.3V

The frame supplies are measured after the module fuses and filtering.

6.3 On-site re-programming

The module may be re-programmed on site with a GYDA Multicon system controller. Firmware will be provided by Neviaon support when necessary.

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
 - Operating room temperature range: 0°C to 45°C
 - Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:
 - Temperature range: -10°C to 55°C
 - Relative humidity range: <90% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the “Administrative Measure on the Control of Pollution by Electronic Information Products”. In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

組成名稱 Part Name	Toxic or hazardous substances and elements					
	鉛 Lead (Pb)	汞 Mercury (Hg)	鎘 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
ADC-AES8	○	○	○	○	○	○
<p>O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.</p> <p>X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.</p>						

This is indicated by the product marking:



A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site <http://www.nevion.com/>. Please contact Nevion’s Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.